

PROJECT NAME : BAL23
PCB NO : LA-D804P(Stoney)

Dell / Compal Confidential

Schematic Document

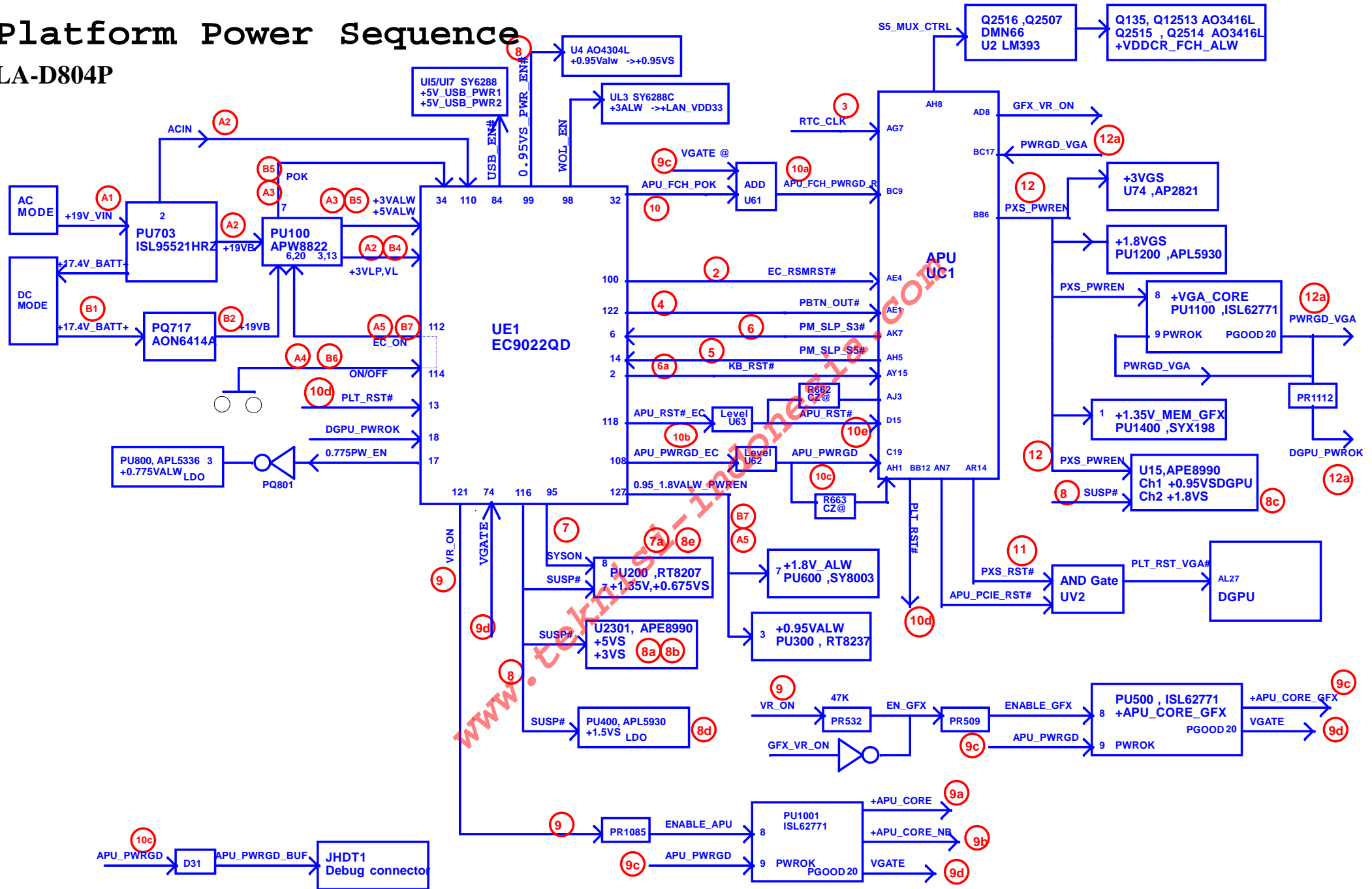
AMD Stoney FT4
AMD R16M-M30 (23 X 23mm) +GDDR5 x2

2016-6-17 Rev: 1.0(A00)

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/06/10	Deciphered Date	2015/06/30	Title	Cover Page	
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Platform Power Sequence

LA-D804P



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Issued Date	2014/06/10	Deciphered Date	2015/06/30	Title		Power Sequence diagram	
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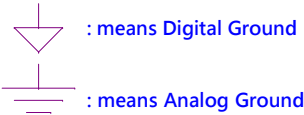
Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	DIMM	APU	GPU	Thermal Sensor		
EC_SMB_CK1 EC_SMB_DA1	KB9022Q	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9022Q				V	V	V		
EC_I2C_TPCLK EC_I2C_TPDAT	KB9022Q								
APU_SCLK0 APU_SDAT0	APU			V					
APU_SCLK1 APU_SDAT1	APU								
APU_SIC APU_SID	APU						V		

Symbol Note :



BOARD ID Table

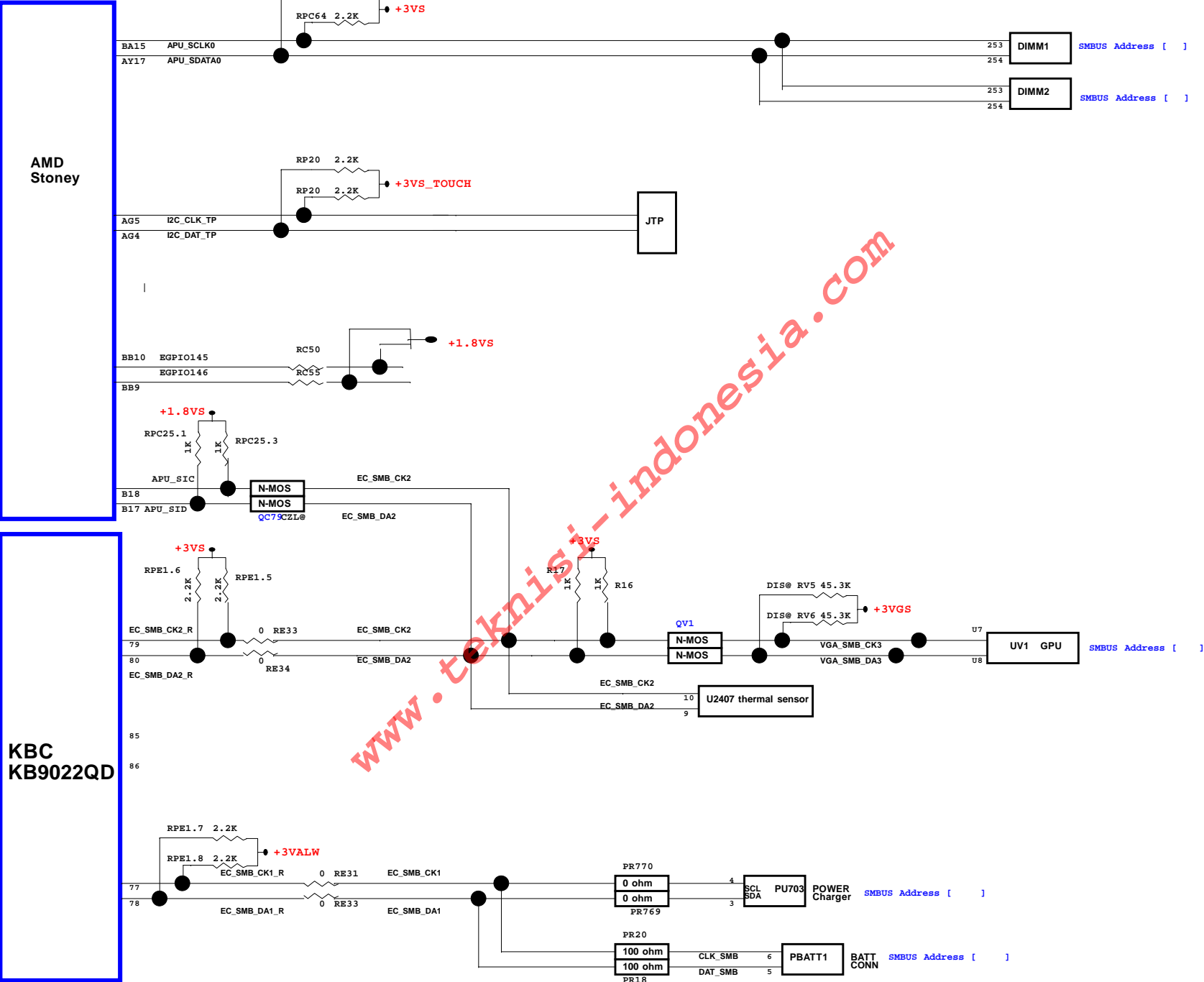
Board ID	
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	BAL23 AMD Stoney DIS EVT
11	BAL23 AMD Stoney UMA EVT
12	BAL23 AMD Stoney DVT1
13	BAL23 AMD Stoney DVT2
14	BAL23 AMD Stoney X build
15	
16	
17	
18	
19	

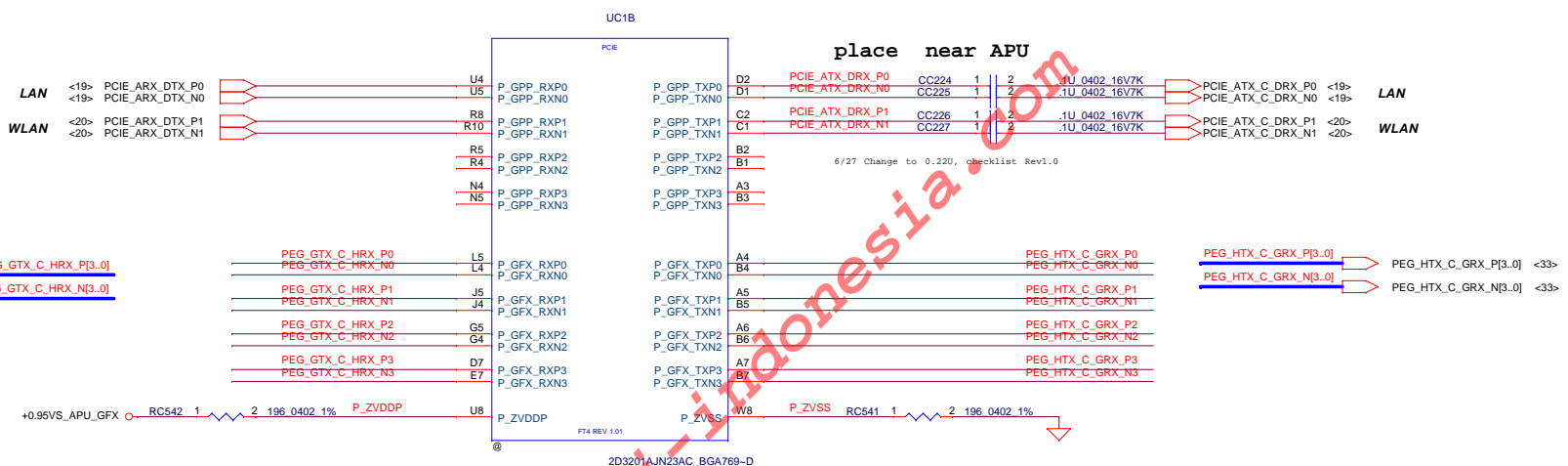
ULT

USB3.0	
Port1	
Port2	USB3 connector 1
Port3	USB3 connector 2
Port4	
USB2.0	
Port0	Card Reader
Port1	Touch Screen Panel
Port2	USB connector 3 (D/B)
Port3	Camera
Port4	NGFF Card (WLAN)
Port5	USB3 connector 1
Port6	USB3 connector 2
Port7	
PCI GPP	
Lane 1	10/100 LAN
Lane 2	NGFF Card (WLAN)
Lane 3	
PCI GFX	
Lane 1	PEG (AMD)EXO UL
Lane 2	PEG (AMD)EXO UL
Lane 3	PEG (AMD)EXO UL
Lane 4	PEG (AMD)EXO UL
SATA	
SATA0	HDD
SATA1	ODD

CLOCK SIGNAL	
CLKOUT_PCIE0	10/100 LAN
CLKOUT_PCIE1	NGFF Card (WLAN)
CLKOUT_PCIE2	
CLKOUT_PCIE3	
GFX CLK	dGPU

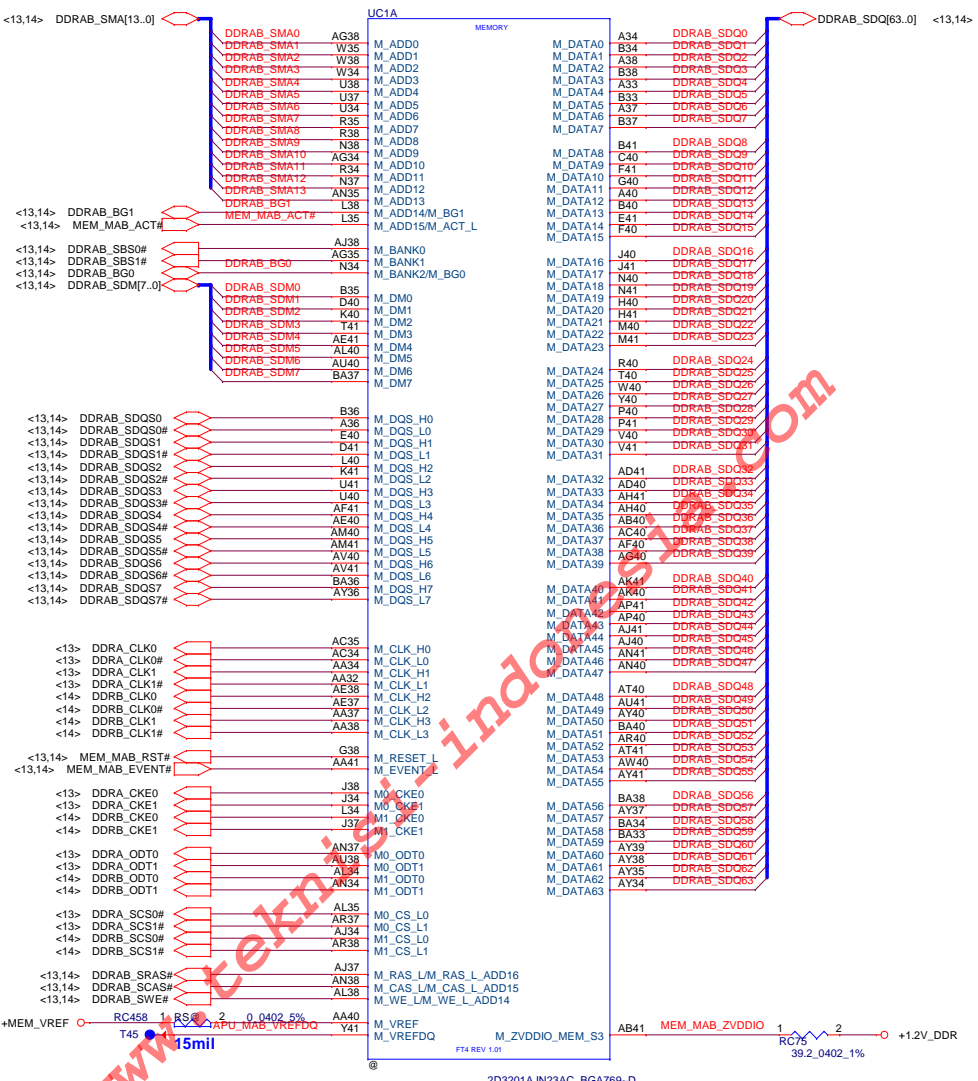
SMBus Block Diagram





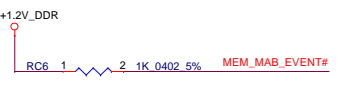
CPU R1 PN	CPU R3 PN
<div>UC1</div> <div>SA0000A2A0L</div> <div>A6_R1@</div> <div>S IC A6-9200 AM9200AKN23AC 2G BGA 769P</div>	<div>UC1</div> <div>SA0000A2A1L</div> <div>A6_R3@</div> <div>S IC A6-9200 AM9200AKN23AC 2G BGA A31!</div>
<div>UC1</div> <div>SA00009W80L</div> <div>E2_R1@</div> <div>S IC E2-9000 EM9000AKN23AC 1.8G BGA 769P</div>	<div>UC1</div> <div>SA00009W81L</div> <div>E2_R3@</div> <div>S IC E2-9000 EM9000AKN23AC 1.8G BGA A31!</div>
<div>UC1</div> <div>SA0000A280L</div> <div>A9_R1@</div> <div>S IC A9-9400 AM9400AKN23AC 2.4G BGA 769P</div>	<div>UC1</div> <div>SA0000A281L</div> <div>A9_R3@</div> <div>S IC A9-9400 AM9400AKN23AC 2.4G BGA A31!</div>
<div>UC1</div> <div>SA00009PC1L</div> <div>A99430_R1@</div> <div>S IC A9-9430 2D3201AJN23AC 3.2G BGA 769P</div>	

update CPU R3 PN 5/26

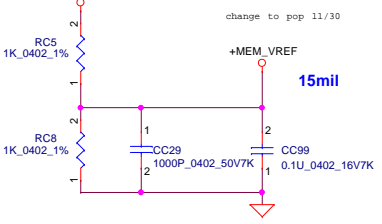


Place them close to APU within 1"

EVENT# pull high



0.6V reference voltage

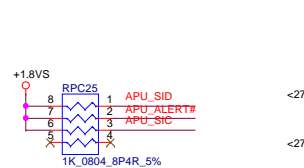
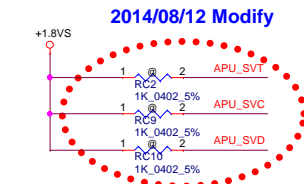
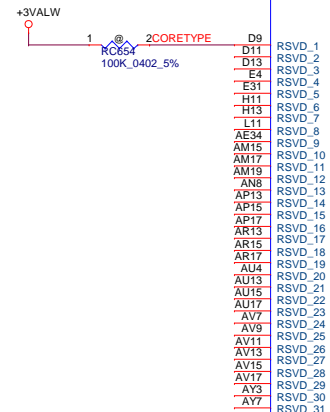
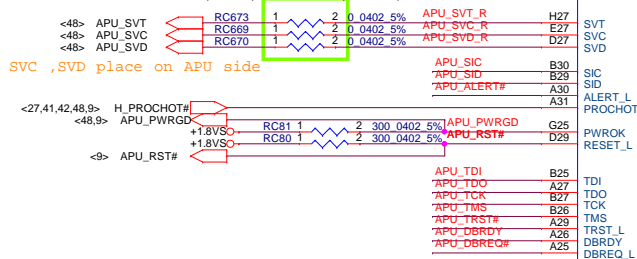


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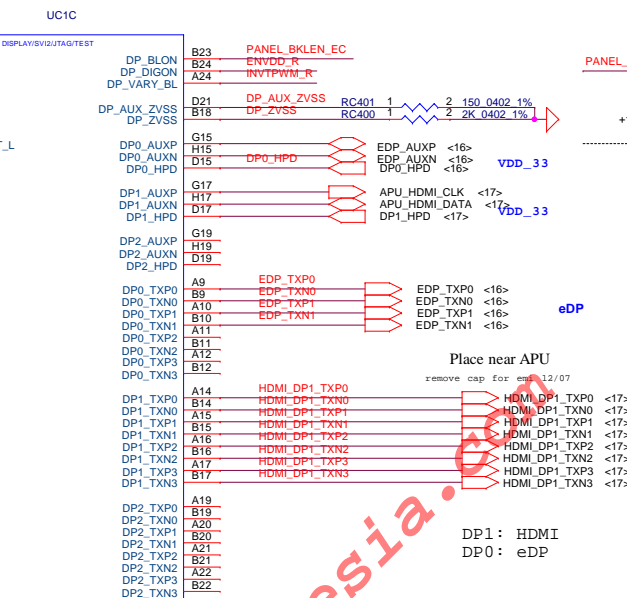
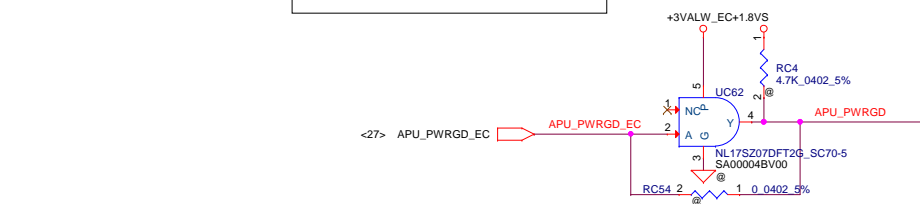
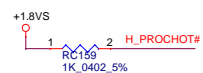
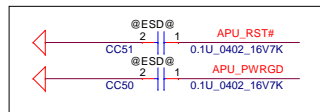
Main Func = CPU

follow DG change to 0-Ω CRB 12/07

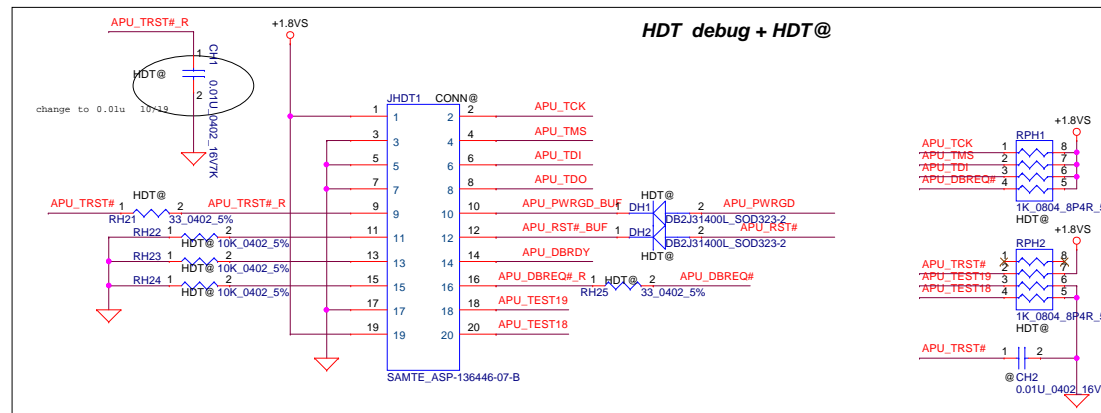
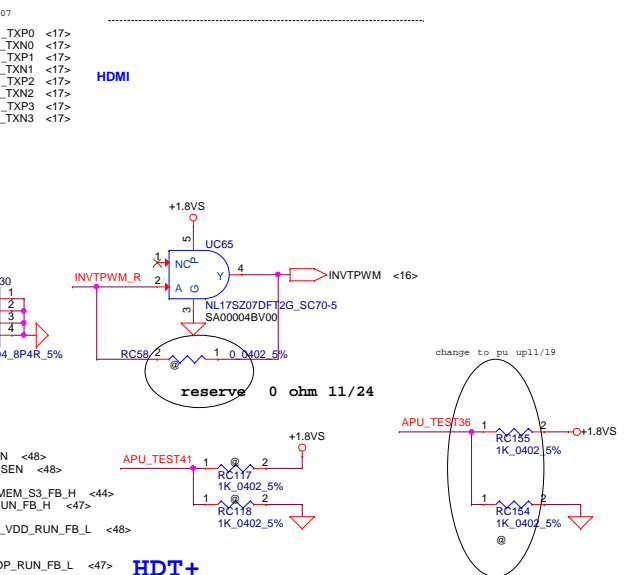
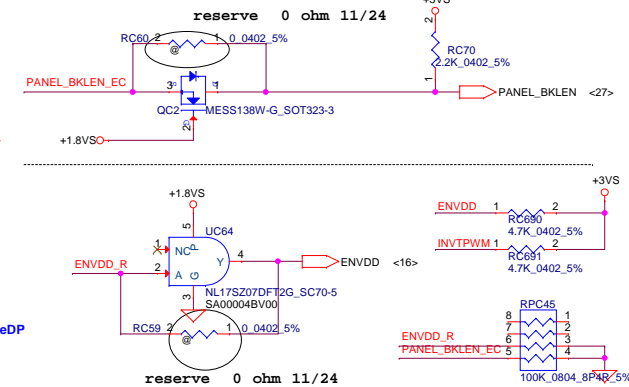
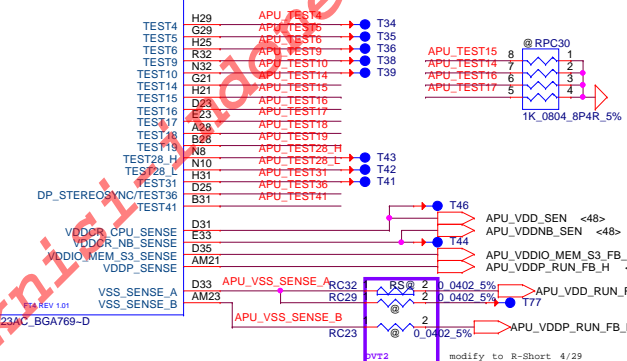
Place resistor(0ohm) for SVT(RC673) on VRM side



PU at EC side

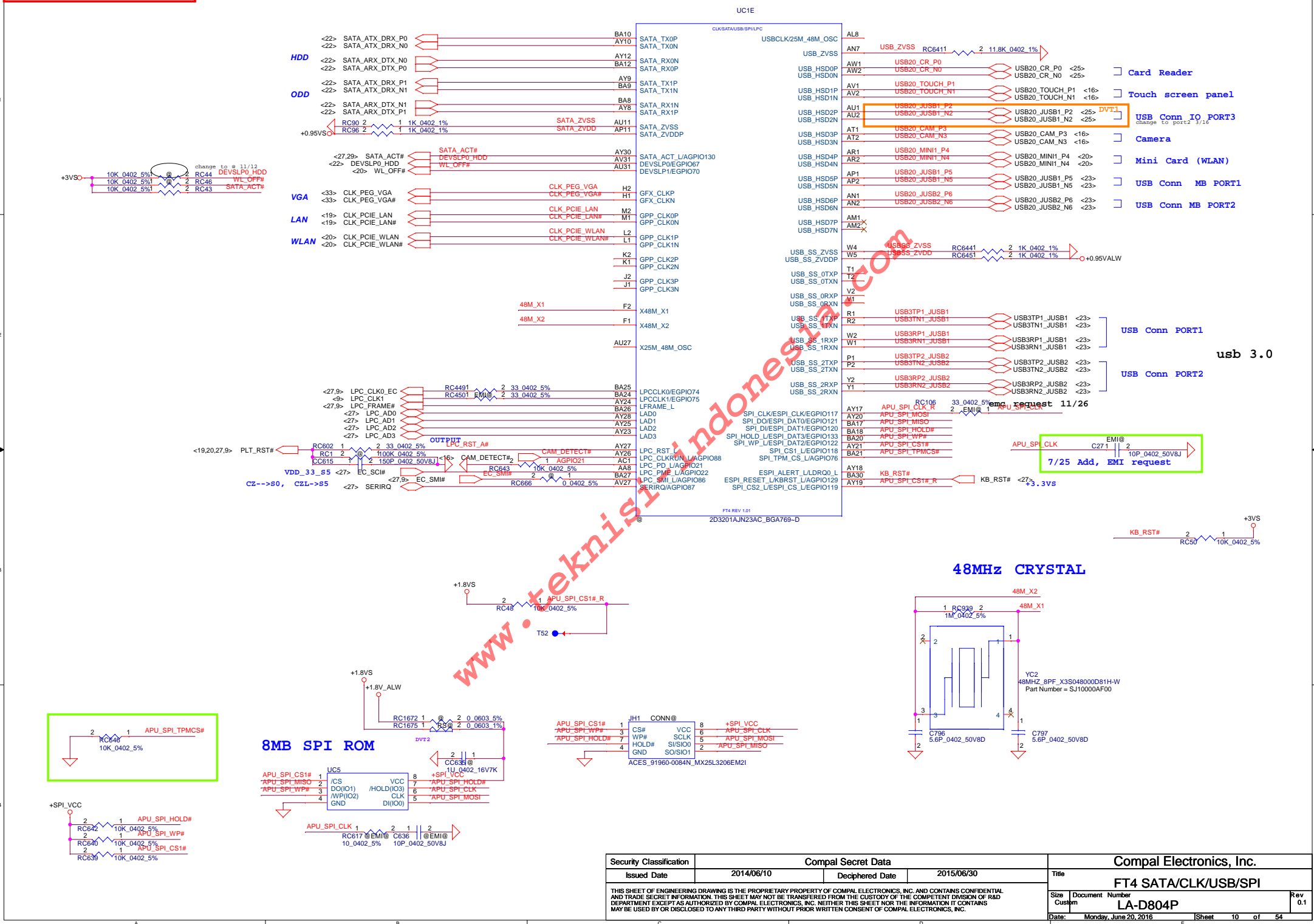


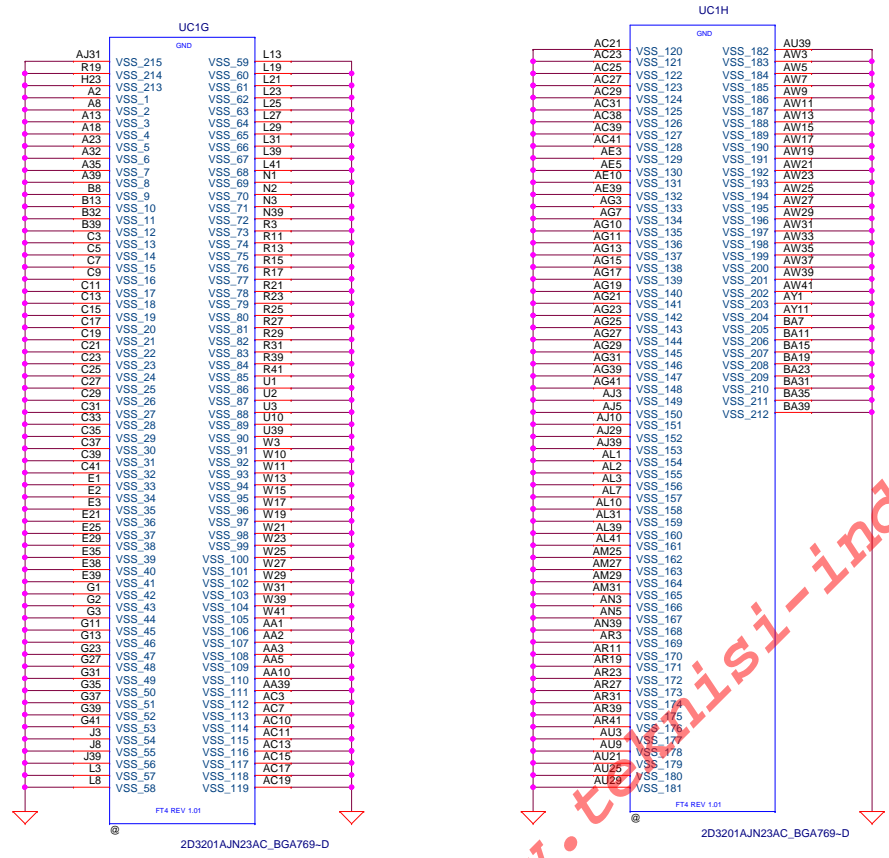
```
DP1: HDMI
DP0: eDP
```



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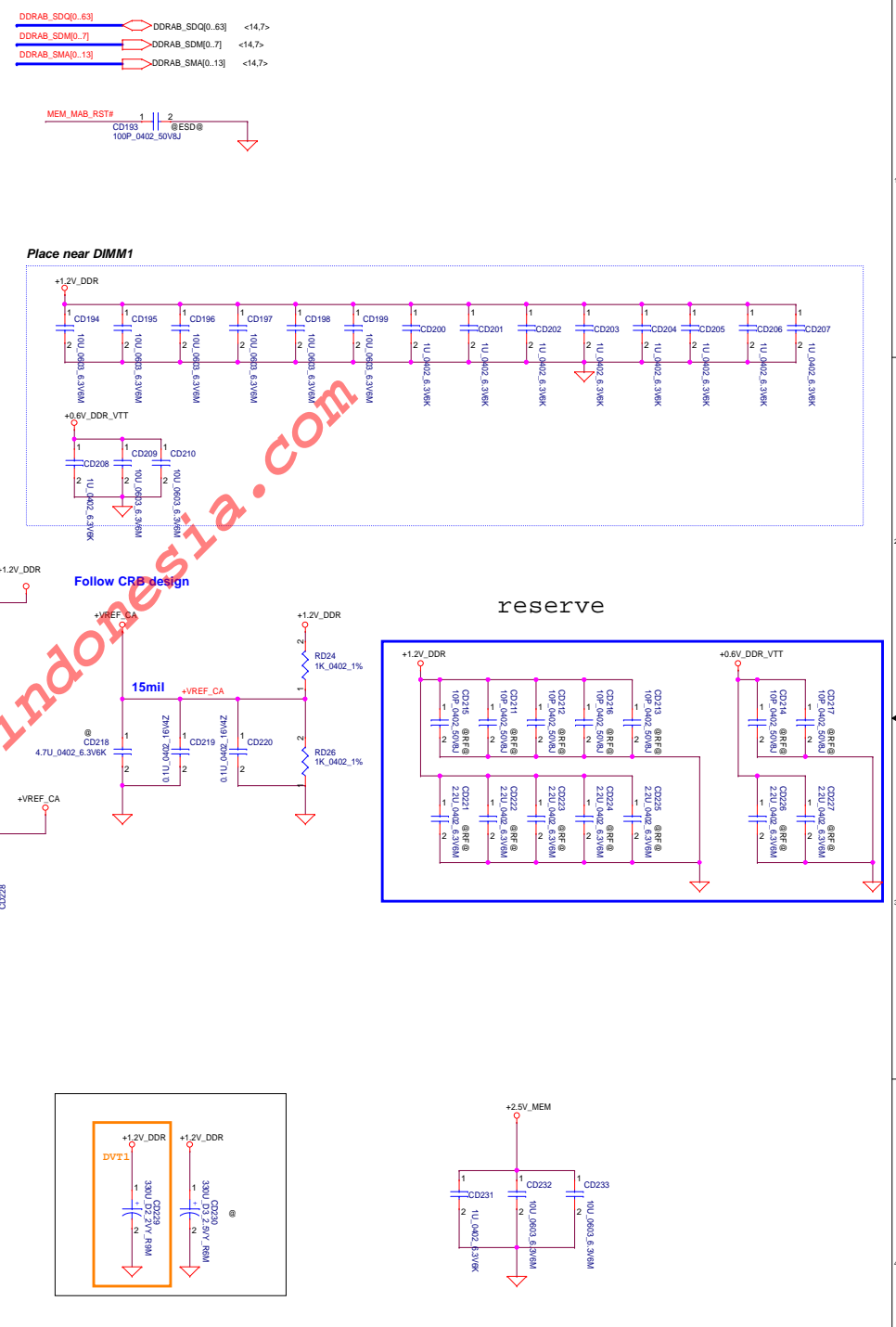
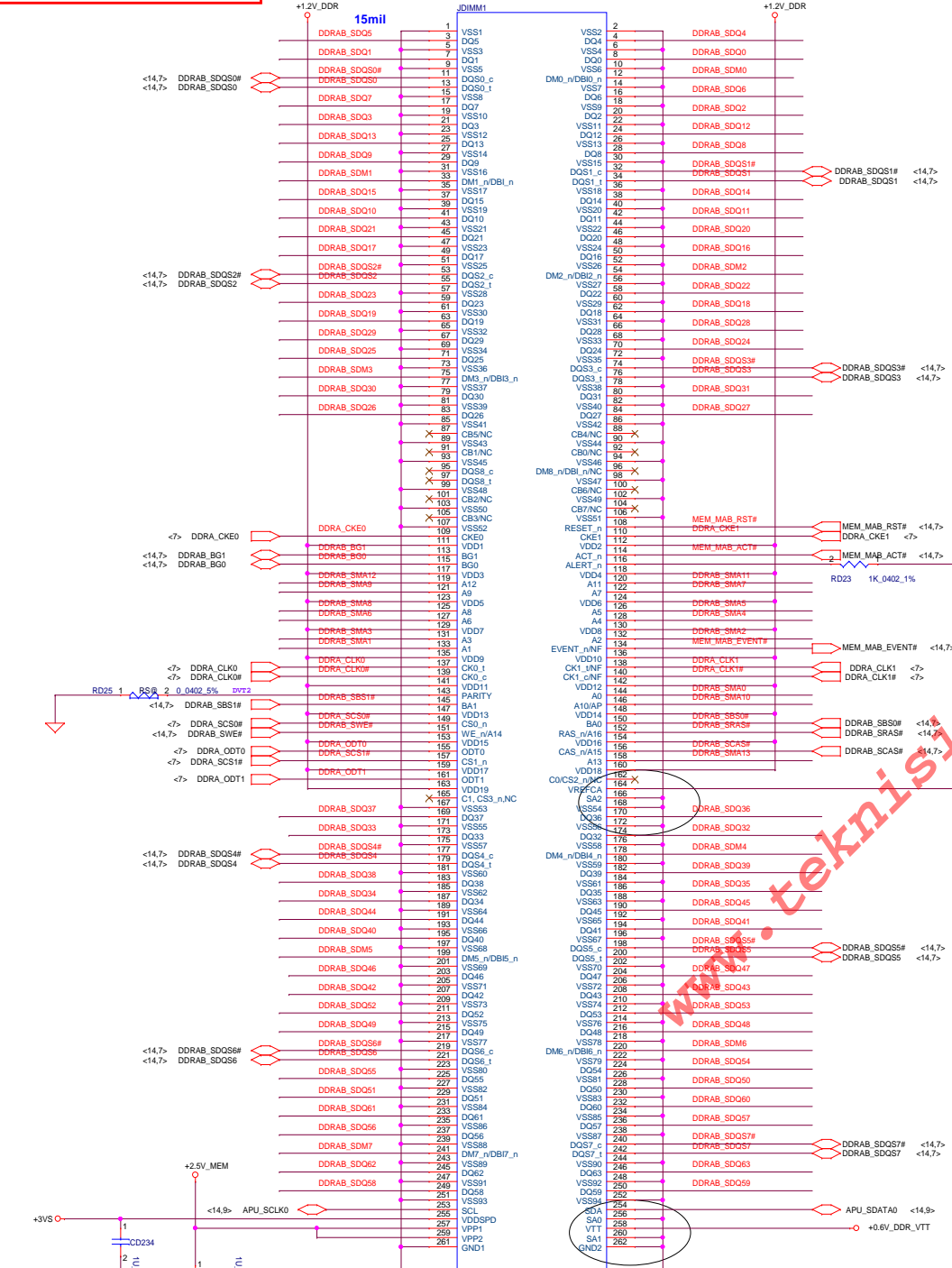
Main Func = CPU



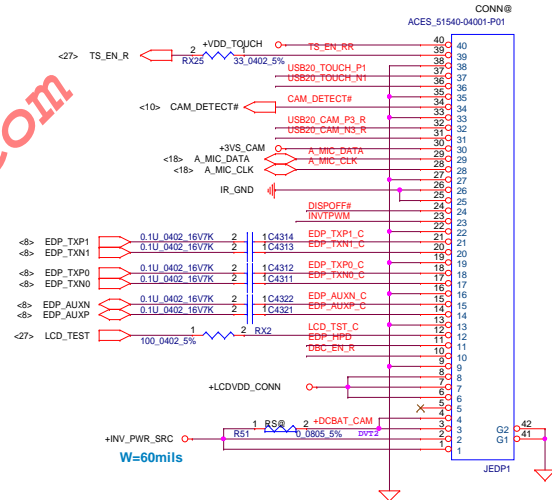
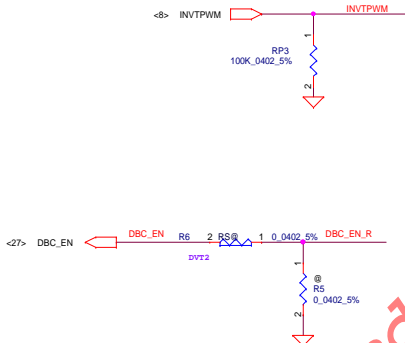
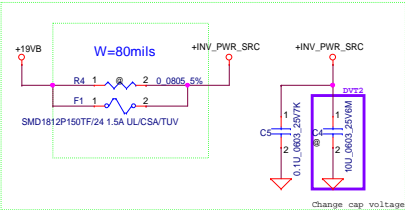
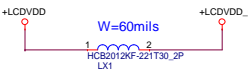
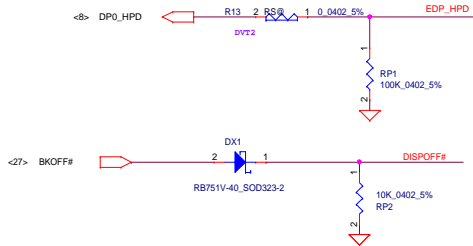
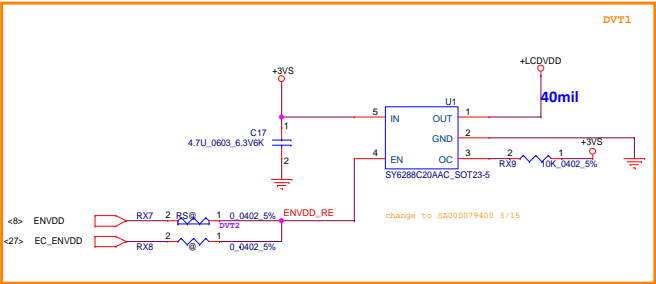


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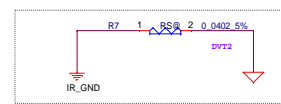
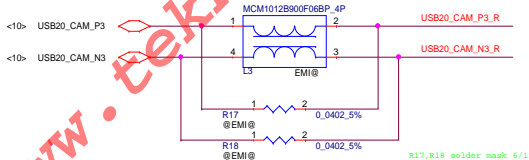
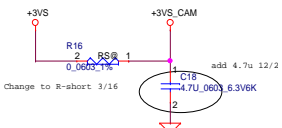
Main Func = DIMM1



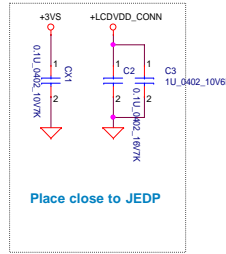
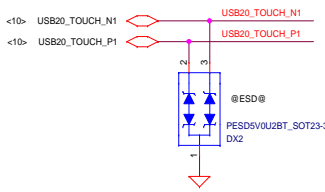
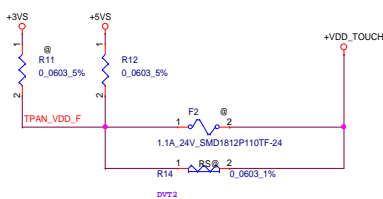
Main Func = LCD



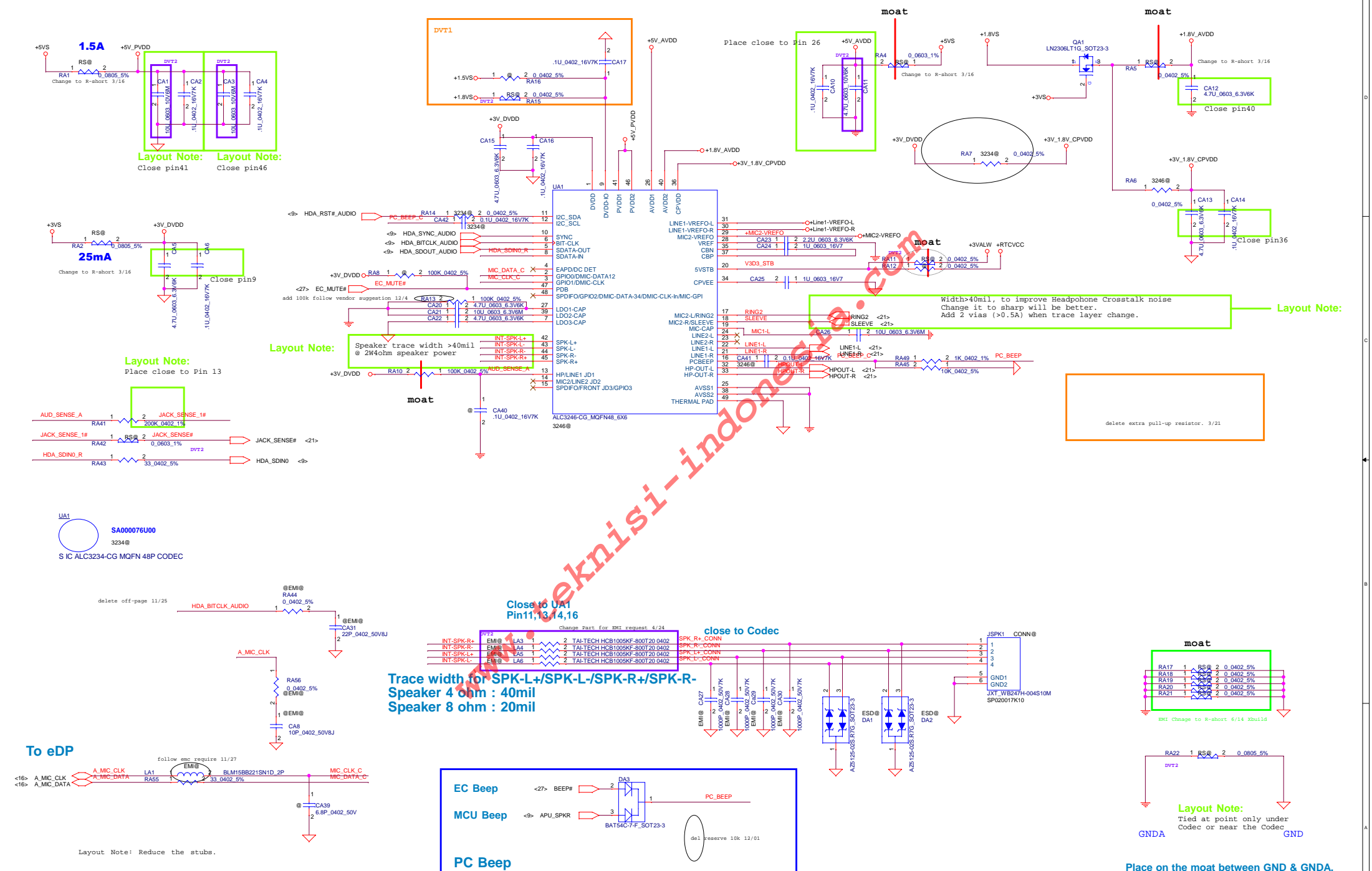
Webcam PWR CTRL



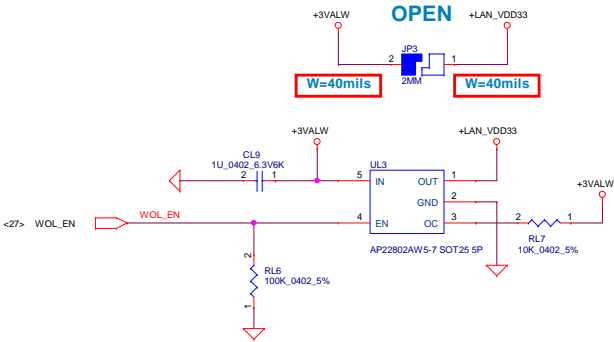
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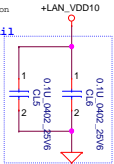
Main Func = Audio



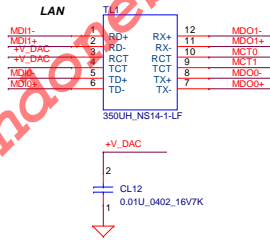
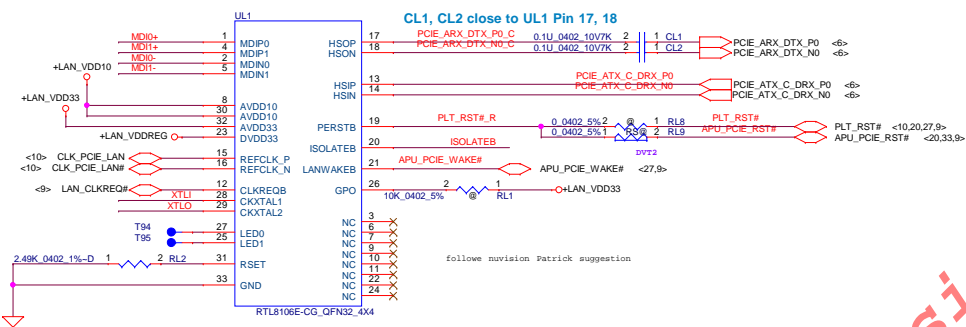
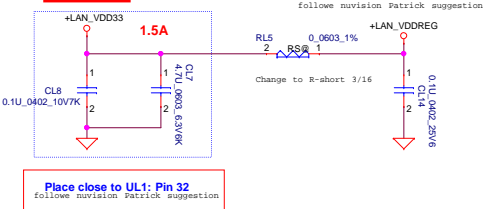
+LAN_VDD33 rising time : >0.5ms and <100ms



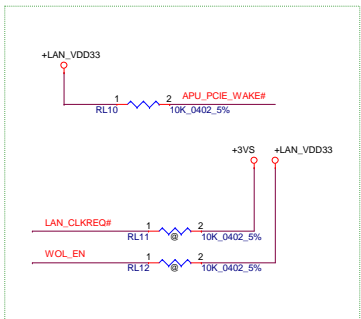
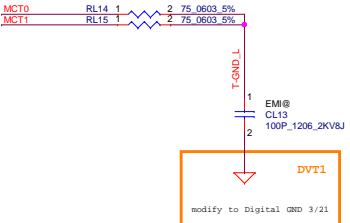
followe nuvision Patrick suggestion
10/100 ethernet design : 20m11



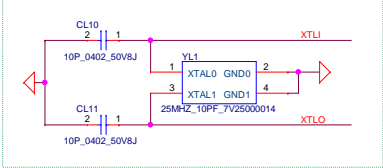
W=40mils



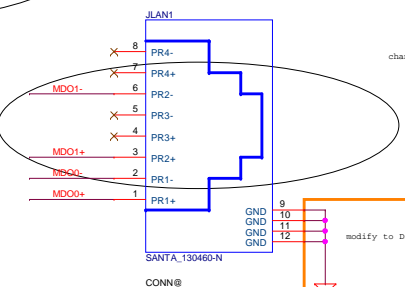
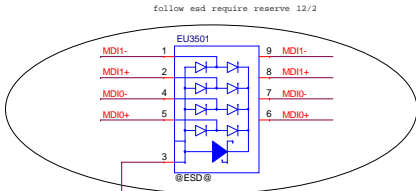
Place close to TCT pin



Reserve 10K pull LAN_IO



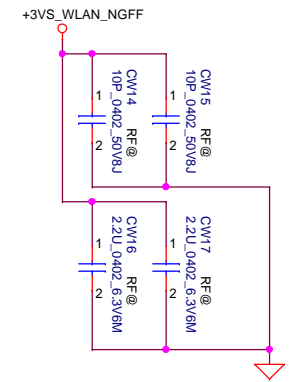
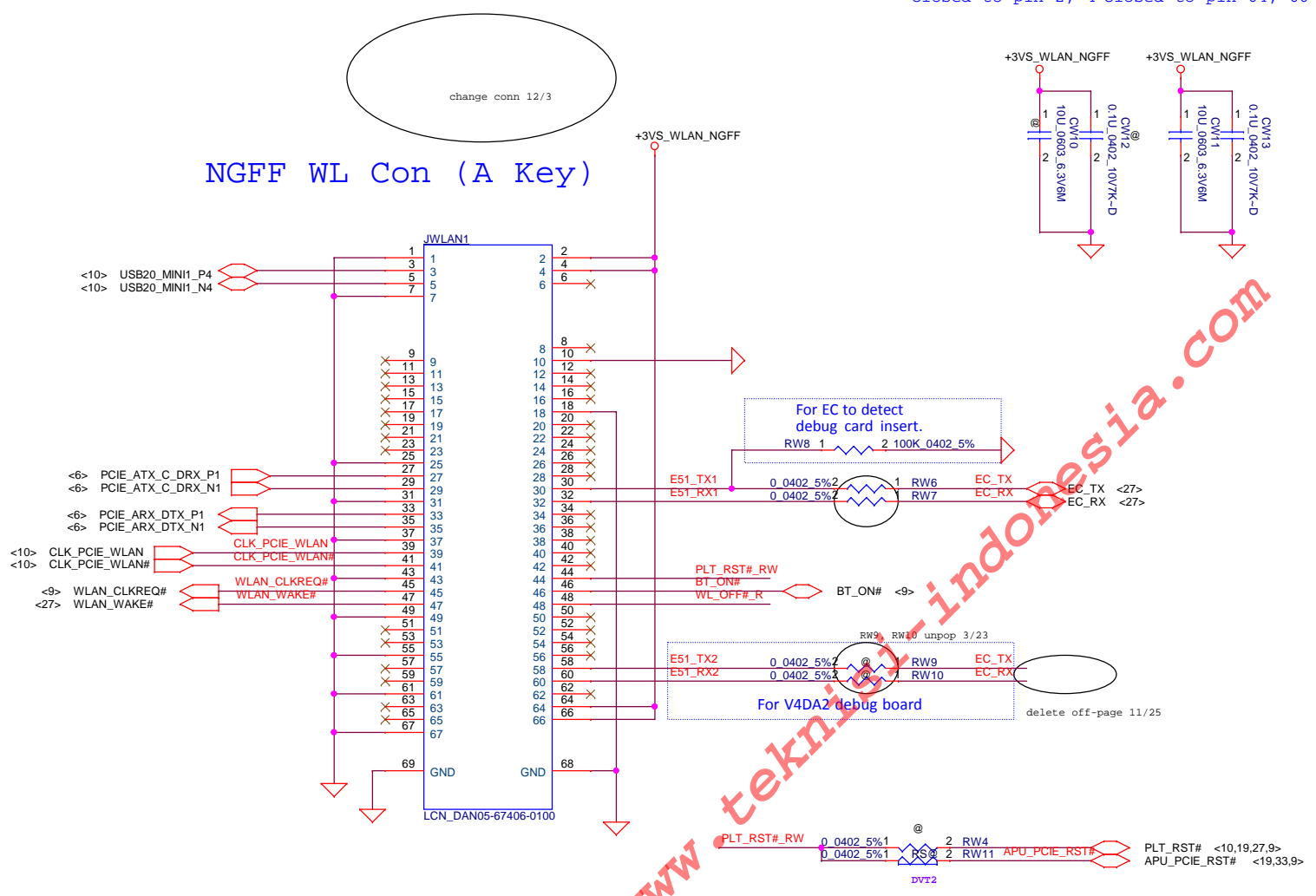
XTAL



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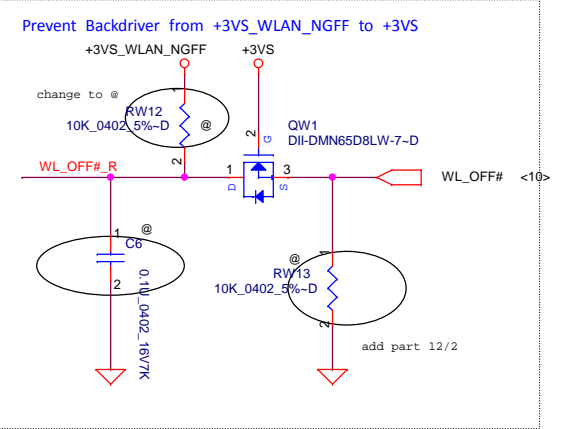
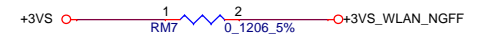
Main Func = WLAN

NGFF WL Con (A Key)



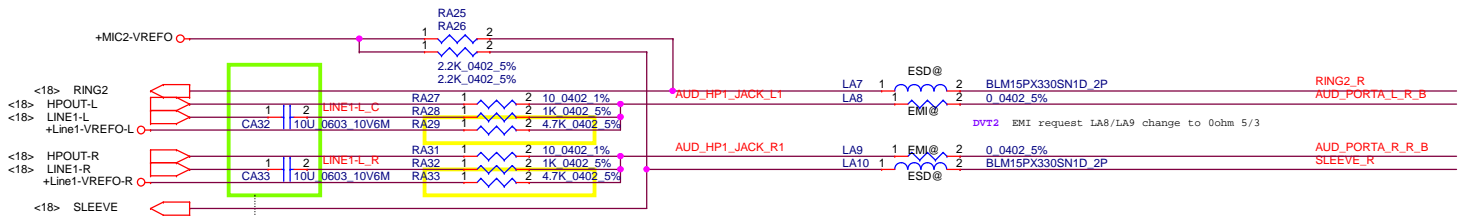
+3VS TO +3VS_WLAN_NGFF

80mil



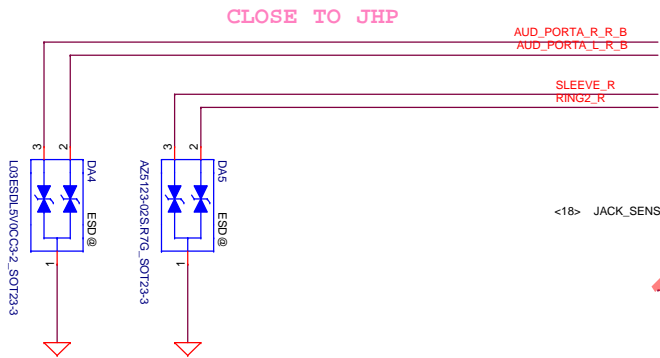
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Main Func = Audio Jack

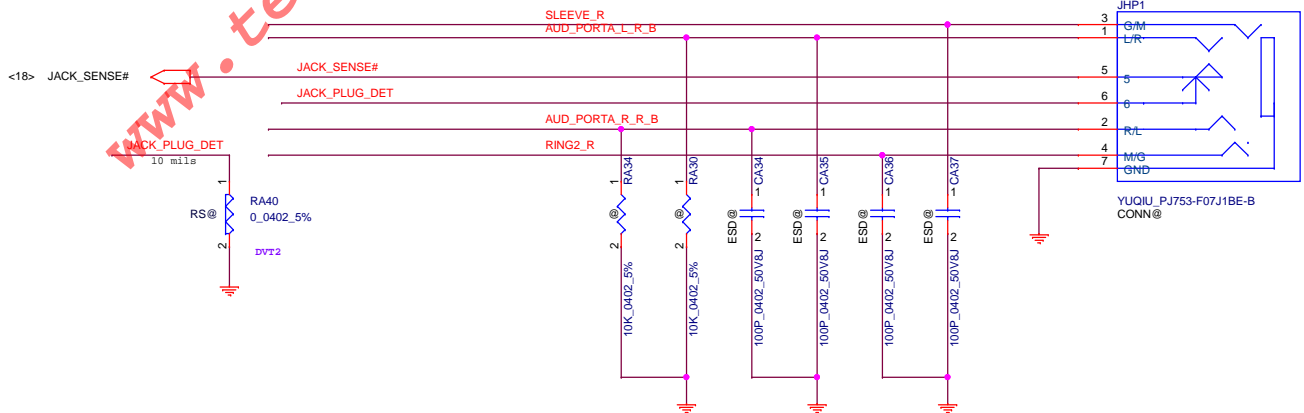


Layout Note:
Close to U1

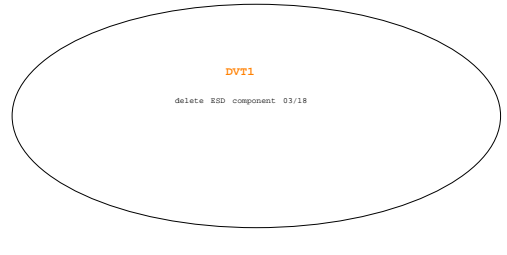
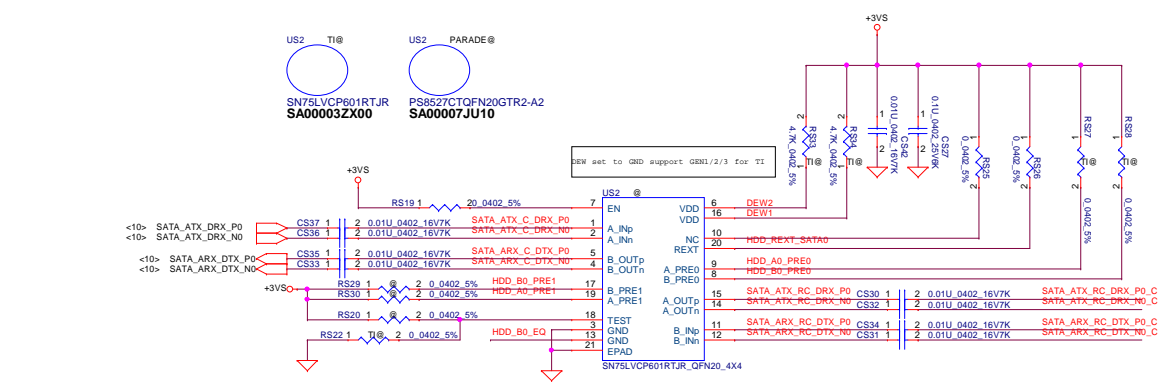
del cap and to place small board 12/1



Universal Jack
(Global Headset Jack + mic phone in + line in support)

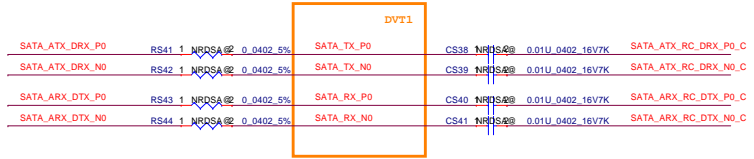


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Size	Document	Number	Rev	LA-D804P	
Date	Monday, June 20, 2016	Sheet	21	of 54	

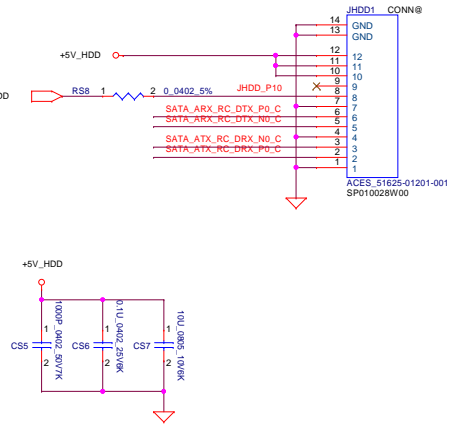


Re-driver EQ setting

Vendor	Part number	RS18	RS22	RS23	RS27	RS28	RS33	RS34	RS37
Parade(M)	SA00007JU10	NC	NC	V	NC	NC	NC	NC	V
TI (2nd)	SA00003ZX00	V	V	V	V	V	4.7K	4.7K	V

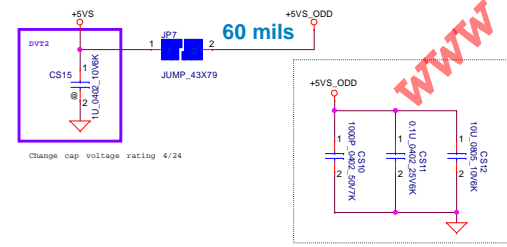


+5V_HDD Source
80 mils
SHORT



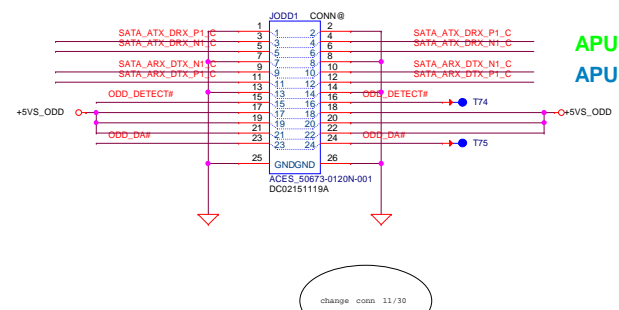
ODD Power Control

need short 11/30



SOC TX
SOC RX

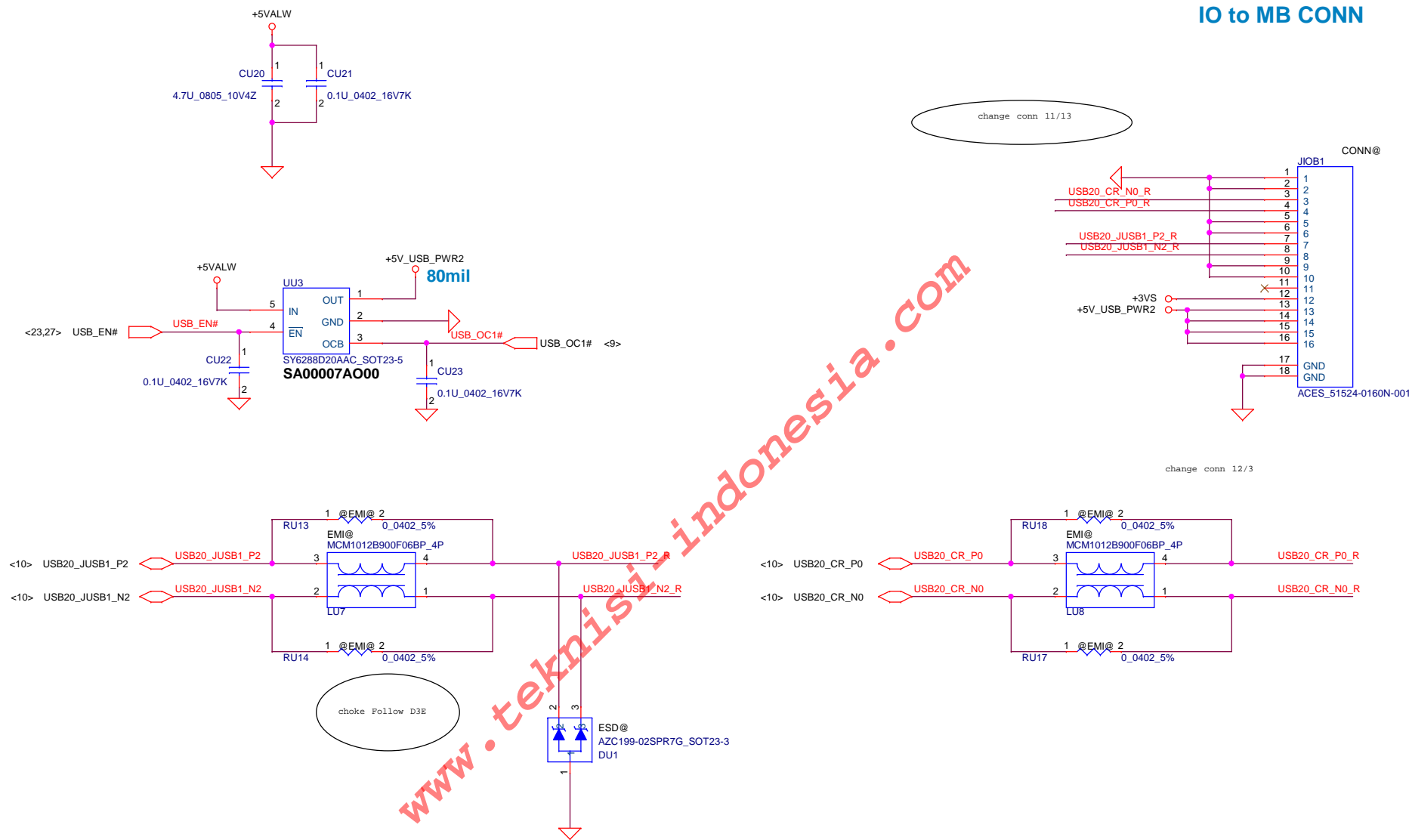
SATA ODD Connector (FFC Type)



APU TX
APU RX

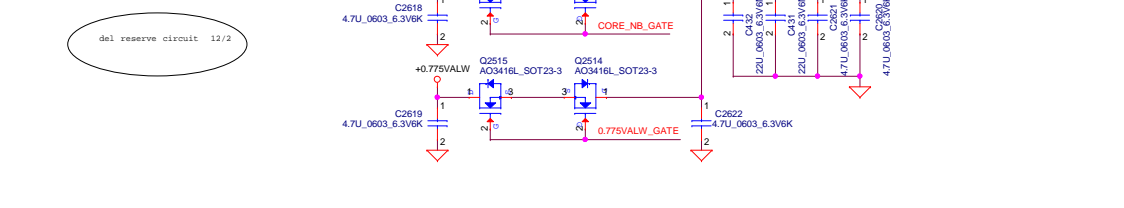
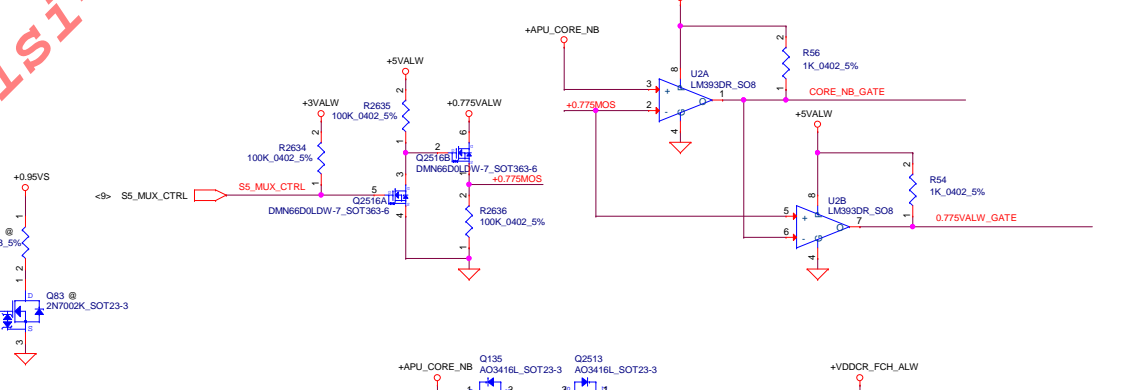
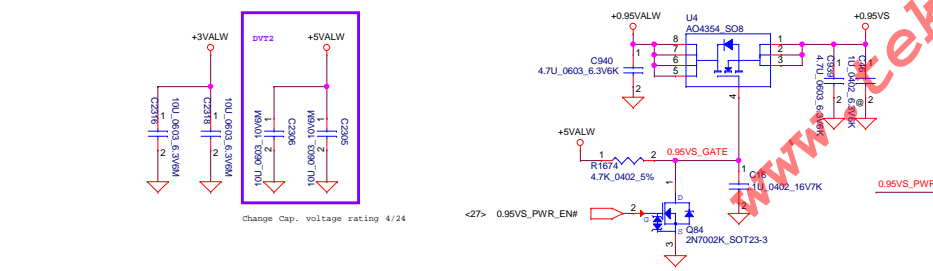
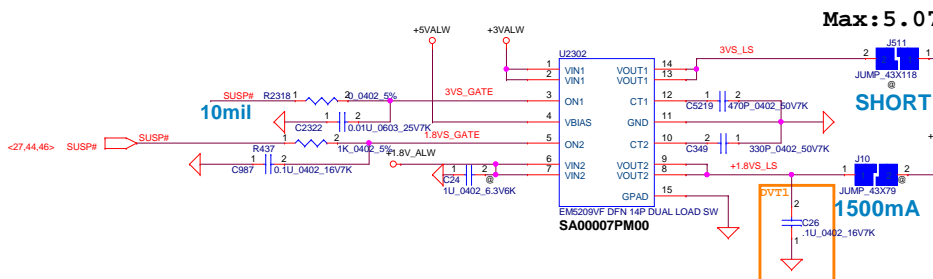
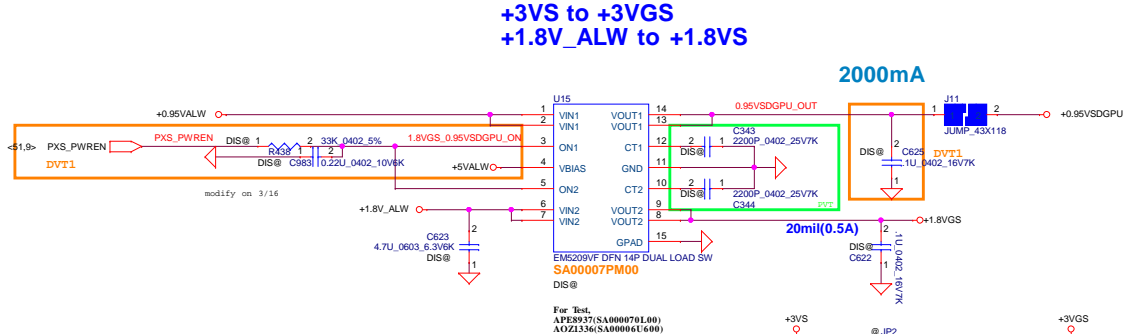
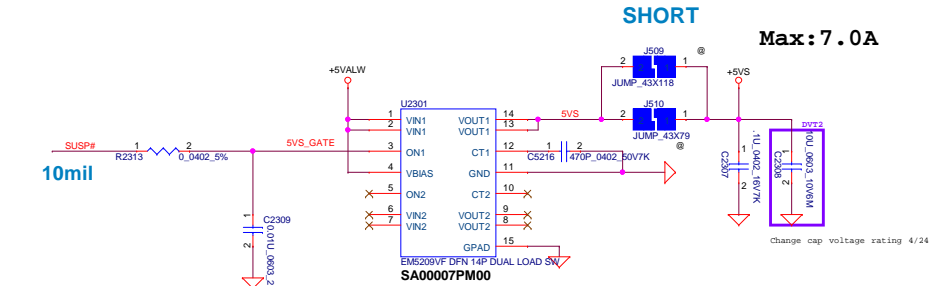
Main Func = IO Connector

IO to MB CONN



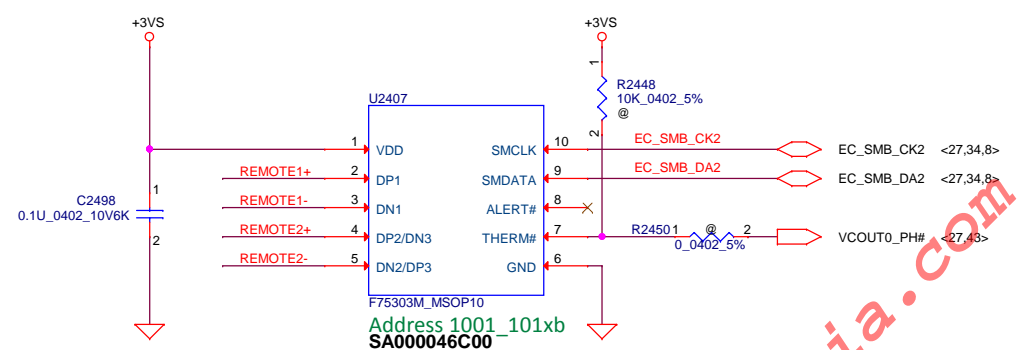
Security Classification		Compal Secret Data		Title	
Issued Date	2014/06/10	Deciphered Date	2015/06/30	IO-DB	
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+5VS and +3VS switch

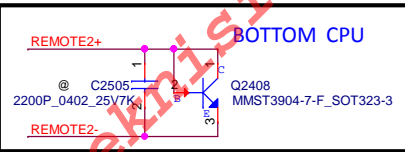
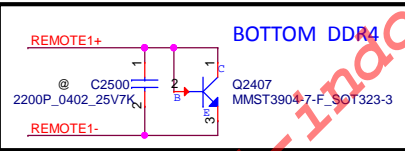
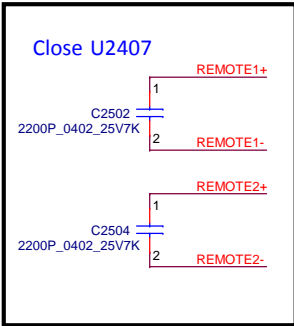


del reserve circuit 12/2

Fintek thermal sensor
placed near by TOP DDR4



2nd source
SA000029210-->EMC1403-2-AIZL-TR

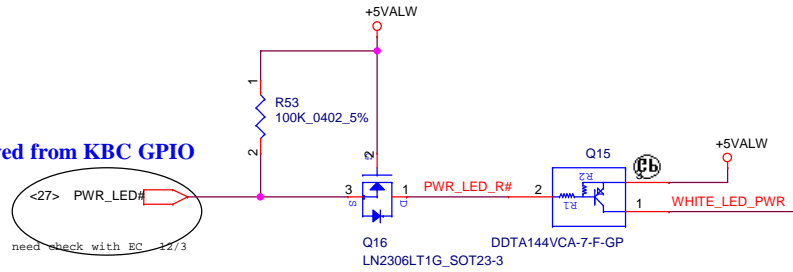


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

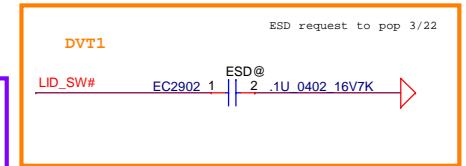
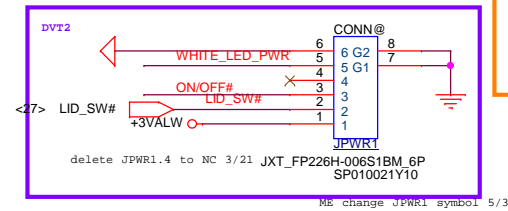
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/06/10	Deciphered Date	2015/06/30	Title	Thermal Sensor
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				LA-D804P	

Main Func = POWER BTN

LOW active from KBC GPIO

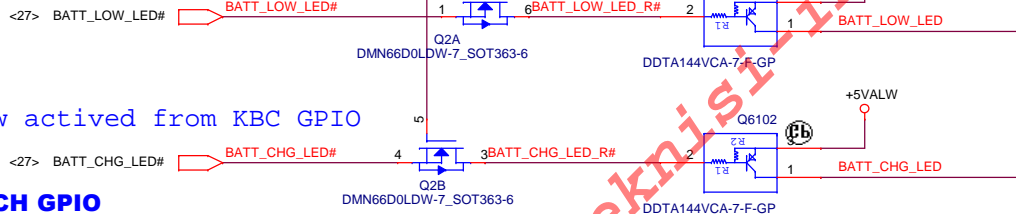


Power button



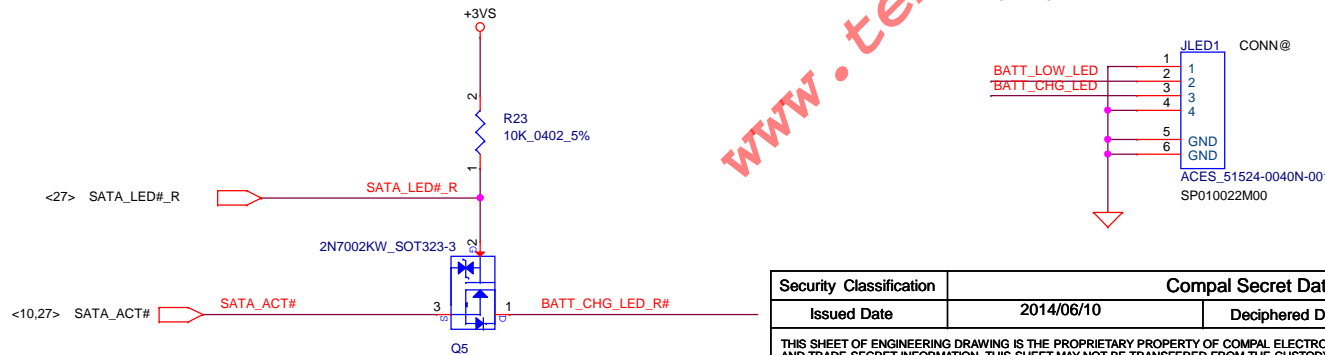
Main Func = Battery BTN

Low active from KBC GPIO



Low active from KBC GPIO

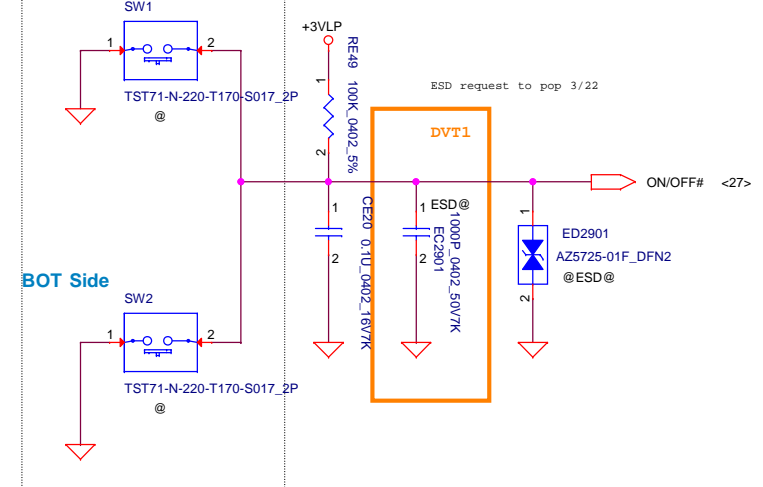
SATA HDD LED
LOW active from PCH GPIO



Pop only before MP

ON/OFF switch

TOP Side



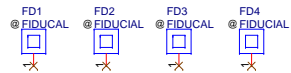
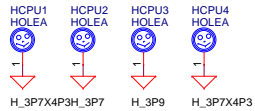
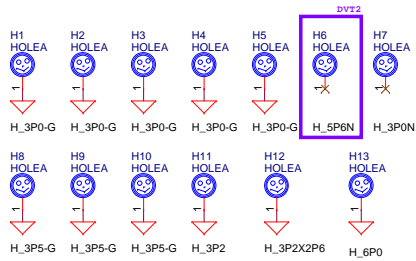
SW1/SW2 Change to SN10000B310

EC2901 must be used 1000pF.

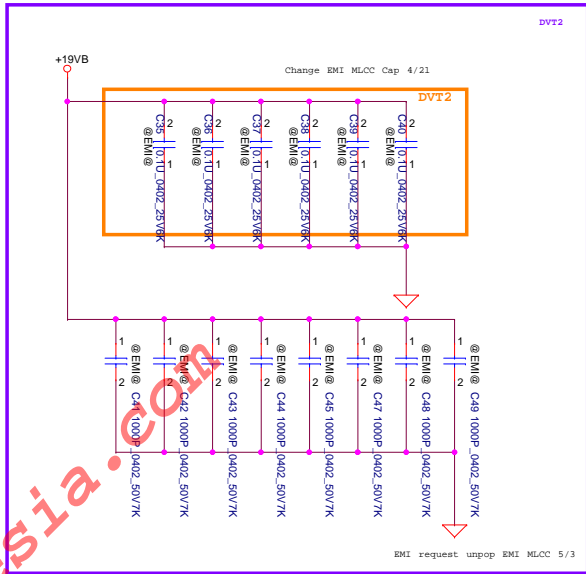
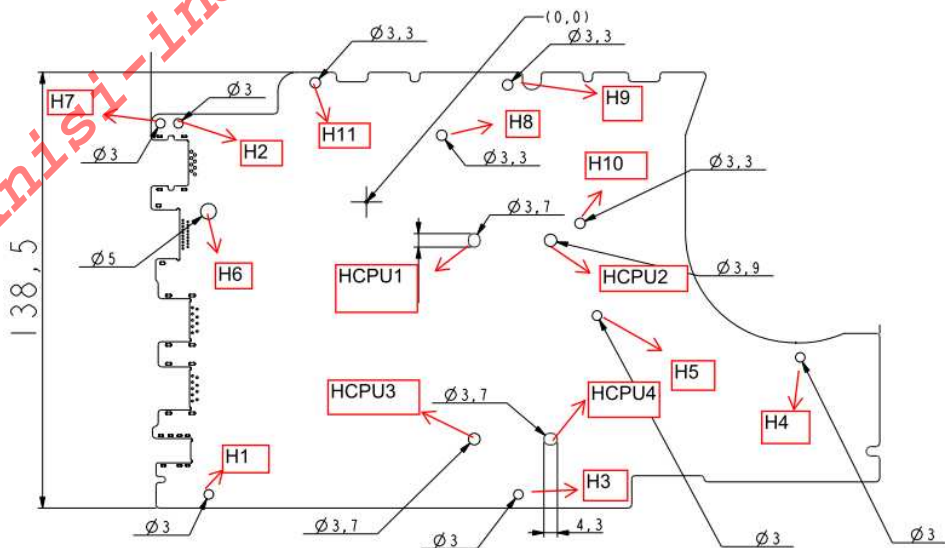
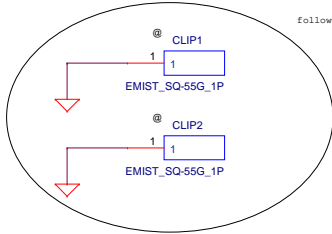
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Issued Date	2014/06/10	Deciphered Date	2015/06/30	Title	Reserved Page
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				Rev	0.1

Main Func = Screw Hole

ZZZ		DVT1
Part Number	Description	
DA6001LB000	PCB 1PG LA-D804P REV0 MB 5	
PCB_R1@		
ZZZ		
Part Number	Description	
DA6001LB011	PCB 1PG LA-D804P REV1 MB GOLD 5 A31.1	
PCB_R3@		



del FD5 FD6 12/1



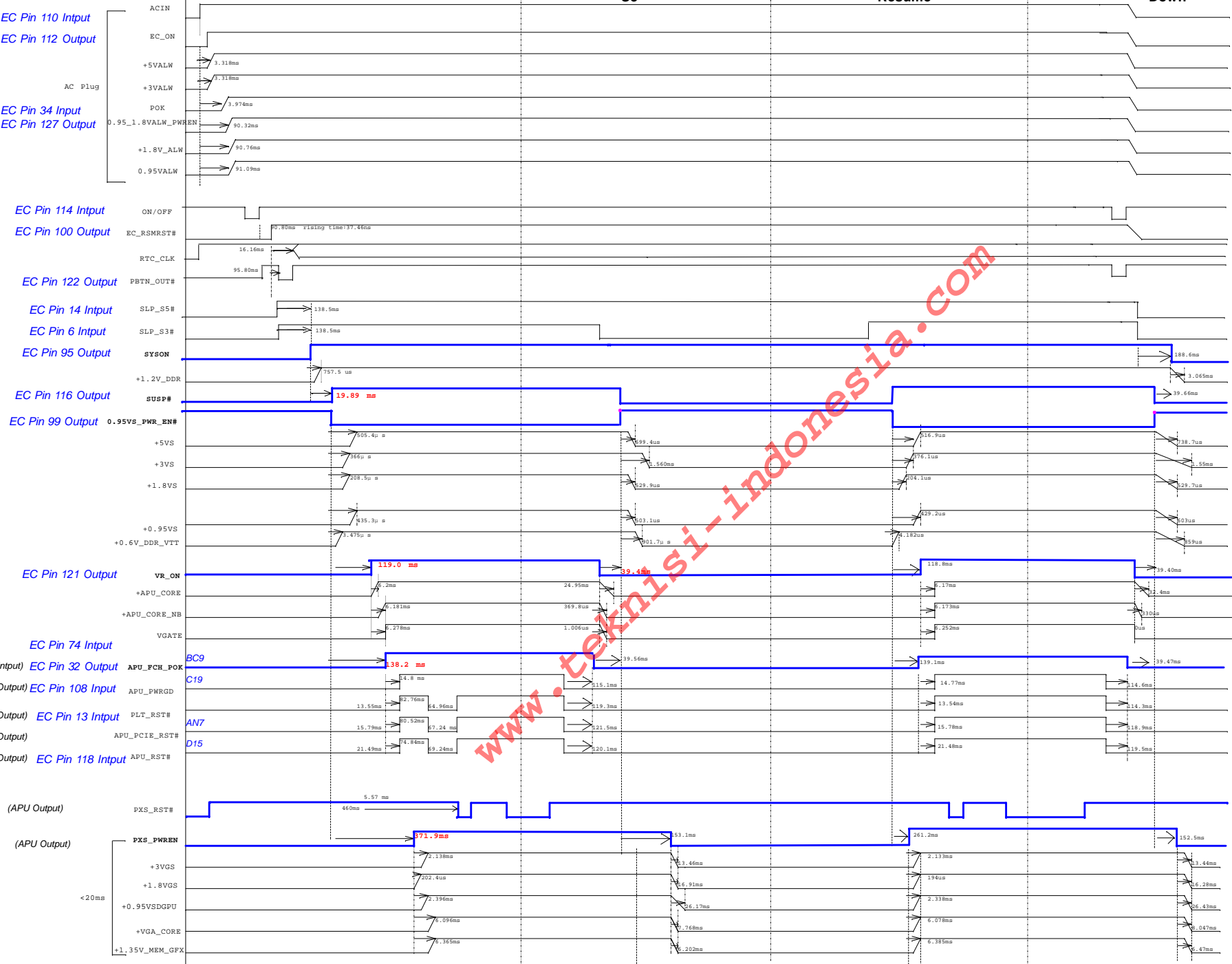
Security Classification		Compal Secret Data		Title	
Issued Date	2014/06/10	Deciphered Date	2015/06/30	Size	Document Number
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SSID1 = TPM2.0

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LA-D804P Power Sequence



<6> PEG_HTX_C_GRX_P[0..3] PEG_HTX_C_GRX_P[0..3]
<6> PEG_HTX_C_GRX_N[0..3] PEG_HTX_C_GRX_N[0..3]
<6> PEG_GTX_C_HRX_P[0..3] PEG_GTX_C_HRX_P[0..3]
<6> PEG_GTX_C_HRX_N[0..3] PEG_GTX_C_HRX_N[0..3]

No Use GPU Display Port output

Add GPU R3 PW 6/14 Xbuild

R16M-M70

UV1

SA000098V0L
M70_R1@
S IC 216-0889-018 A0 R16M-M1-70 FCBGA 631P

UV1

SA000098V1L
M70_R3@
S IC 216-0889-018 A0 R16M-M1-70 A31!

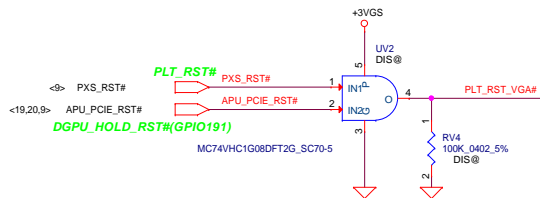
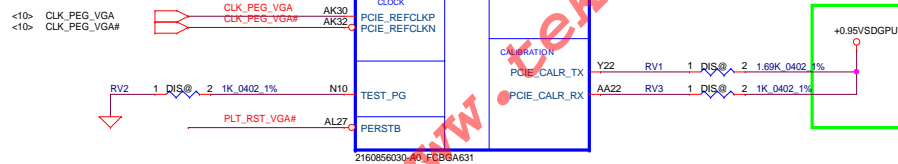
R16M-M30

UV1

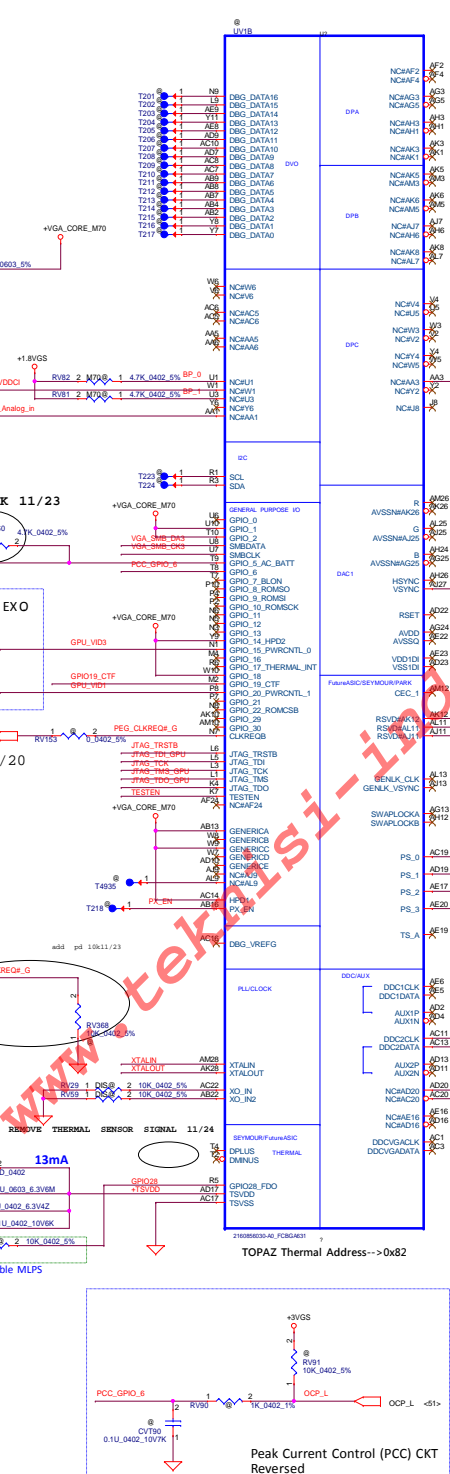
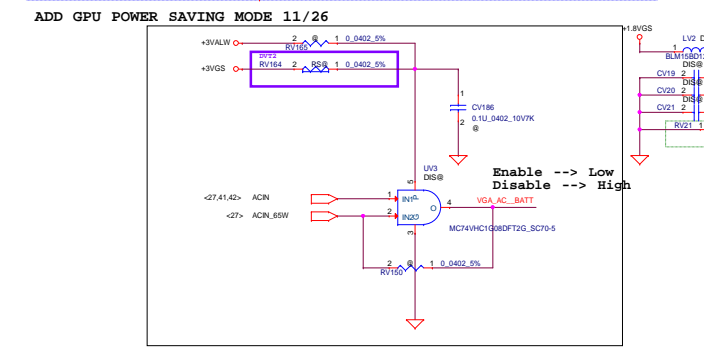
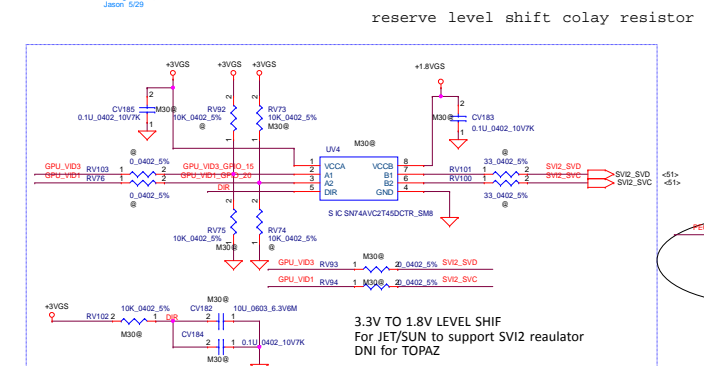
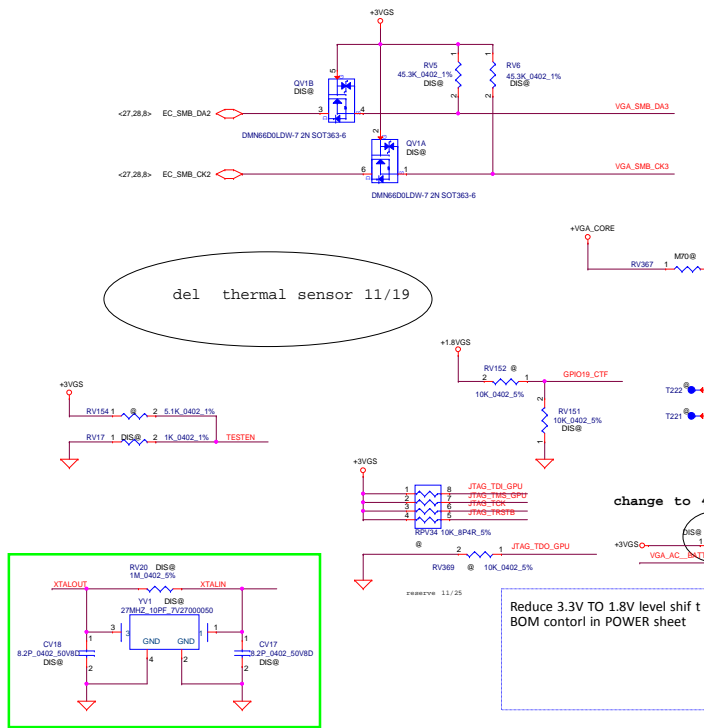
SA000087T0L
M30_R1@
S IC 216-0890-010 A0 R16M-M1-30 FCBGA 631P

UV1

SA000087T2L
M30_R3@
S IC 216-0890-010 A0 R16M-M1-30 A31!



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Resistor Divider Lookup Table

0402 1% resistors are equied

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Table

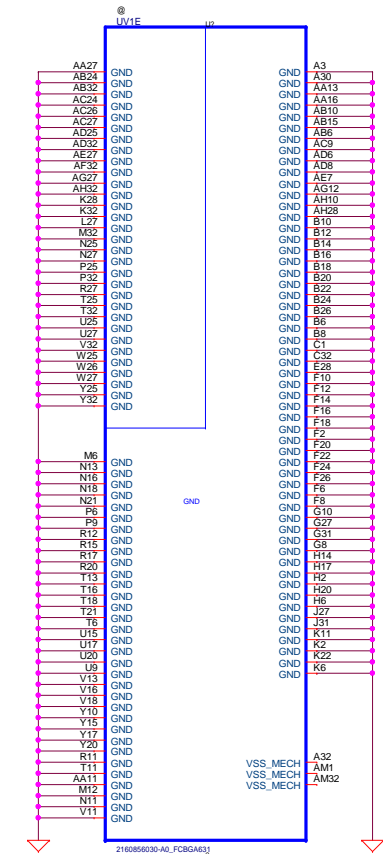
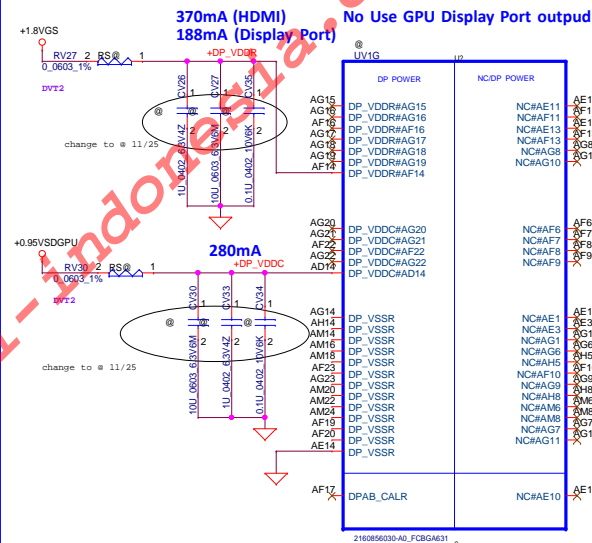
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Strap Name :	Strap Name :	Strap Name :	Strap Name :
PS_0[3:1]=001 PS_0[5:4]=11	PS_0[1] ROM_CONFIG[0] PS_0[2] ROM_CONFIG[1] PS_0[3] ROM_CONFIG[2] PS_0[4] N/A PS_0[5] AUD_PORT_CONN_PINSTRAP[0]	PS_1[3:1]=001 PS_1[5:4]=11	PS_1[1] STRAP_BIF_GEN3_EN_A PS_1[2] TRAP_BIF_CLK_PM_EN PS_1[3] N/A PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000 PS_2[5:4]=11	PS_2[1] N/A PS_2[2] N/A PS_2[3] STRAP_BIOS_ROM_EN PS_2[4] STRAP_BIF_VGA_DIS PS_2[5] N/A	PS_3[3:1]=000 PS_3[5:4]=11	PS_3[1] BOARD_CONFIG[0] (Memory ID) PS_3[2] BOARD_CONFIG[1] (Memory ID) PS_3[3] BOARD_CONFIG[2] (Memory ID) PS_3[4] AUD_PORT_CONN_PINSTRAP[1] PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

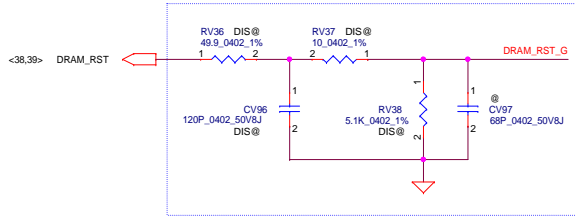
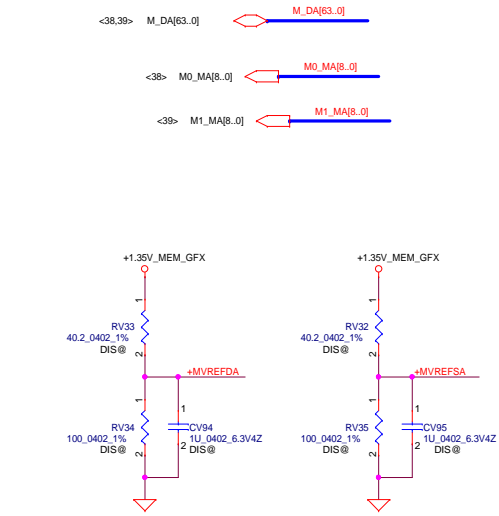
VRAM Type
Need reference
X76 Schematic

Boot-VID Code

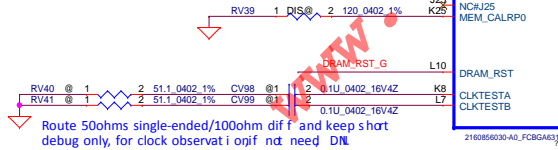
SVc	SVd	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



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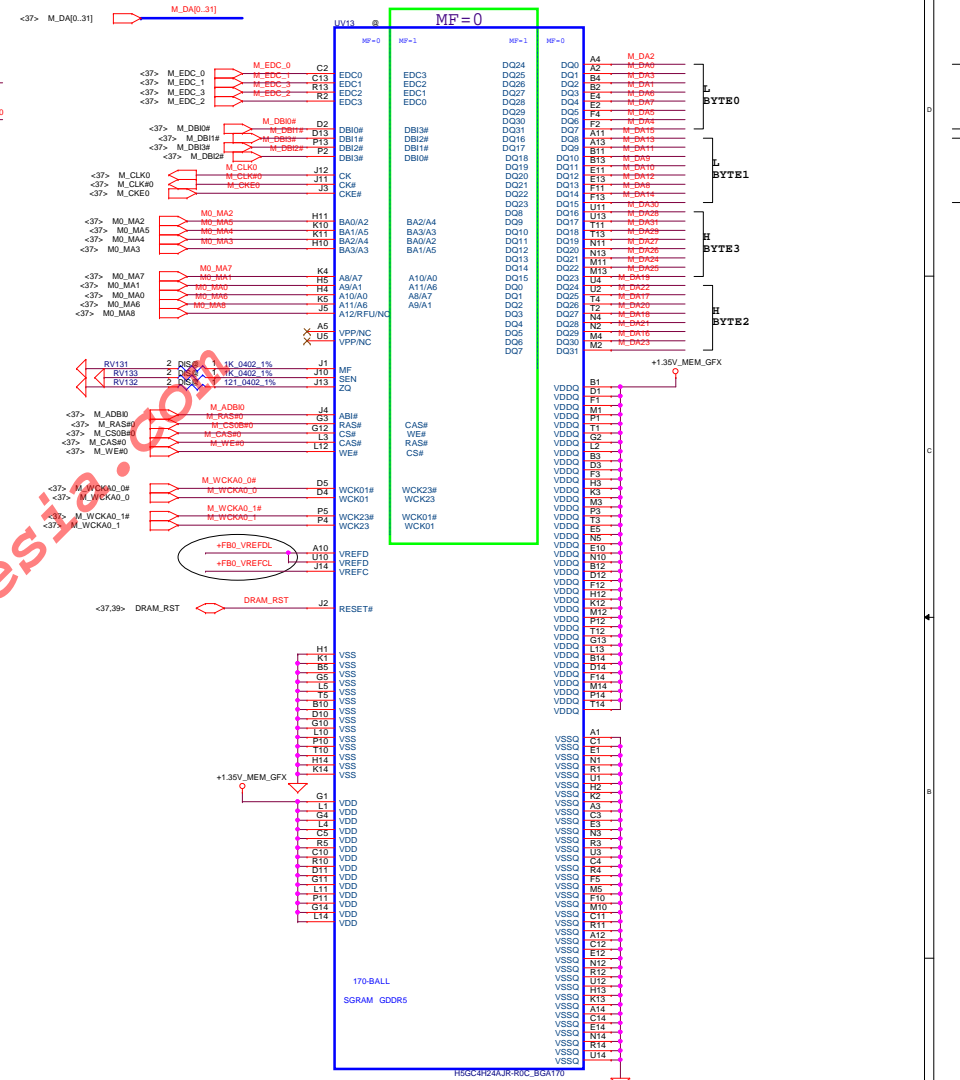
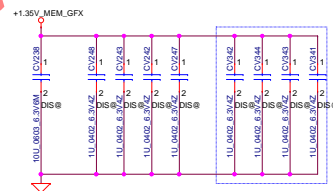
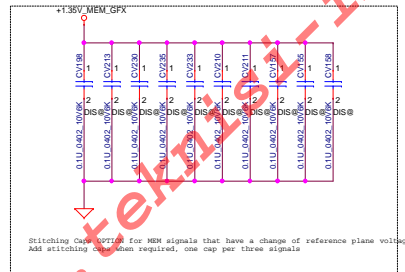
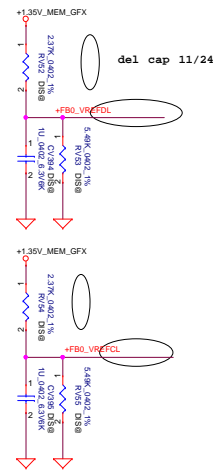
Place close to GPU (within 25mm)
and place component within (5mm) close to each other



Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observat on if not need DN

		GDDR5/D0R3				GDDR5/D0R3																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
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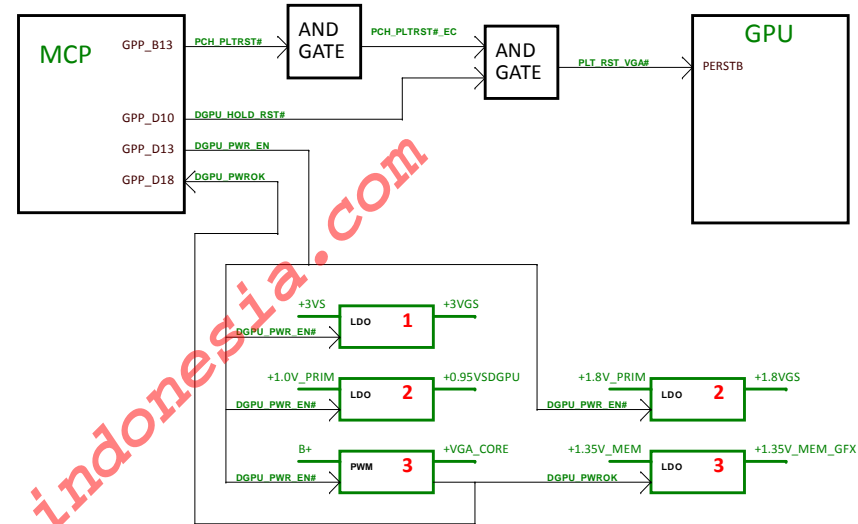
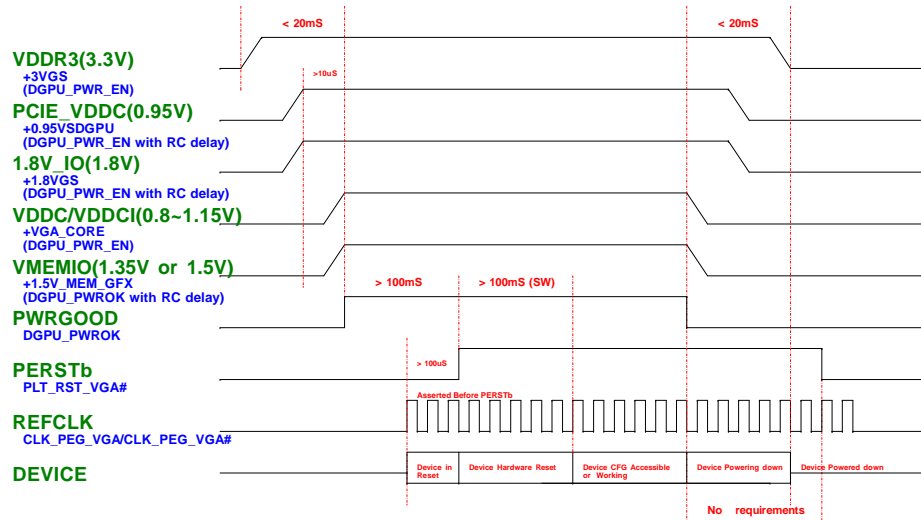
VRAM R1 PN		VRAM R3 PN	
UV13	SA000092D0L S2G_R1#	UV13	SA000094R1L S2G_R3#
S IC D5 256M32 K4G80325FB-HC28 FBGA 170P		S IC D5 256M32 K4G80325FB-HC03 FBGA A31!	
UV13	SA00009U10L HGQ_R1#	UV13	SA00009U11L HGQ_R3#
S IC D5 256M32 H5G6CH24MJUR-JRC BGA 170P		S IC D5 256M32 H5G6CH24MJUR-JRC BGA A31!	
UV13	SA00009TV0L M2G_R1#	UV13	SA00009TV1L M2G_R3#
S IC D5 256M32 MT51J256M32HF-70-A FBGA		S IC D5 256M32 MT51J256M32HF-70-A A31!	



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Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as 50 mV/ μ s).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.



SAMSUNG 2G (000)	HYNIX 2G (110)	MICRON 2G (111)
RV16 2G_S0 4.75K_0402_1% SD034475180	RV15 2G_H0 3.4K_0402_1% SD034340180	RV16 2G_H0 10K_0402_1% SD034100280
RV15 2G_M0 4.75K_0402_1% SD034475180		

Update on 3/24

Table 3-21 Resistor Divider Lookup T

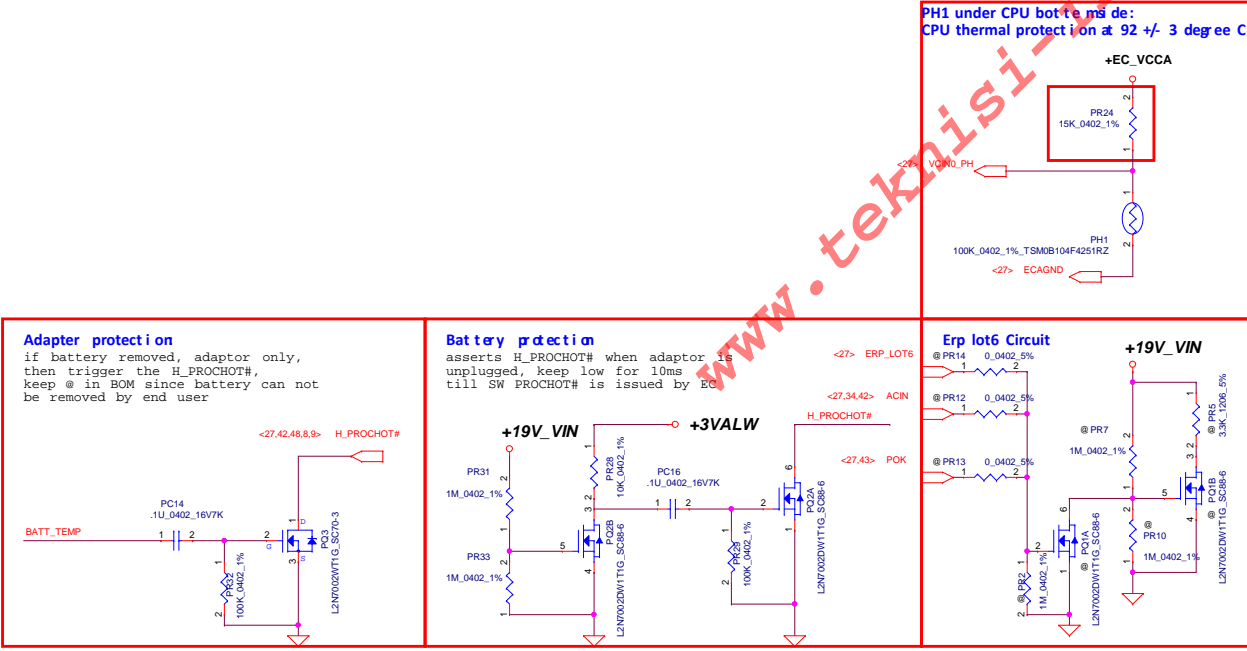
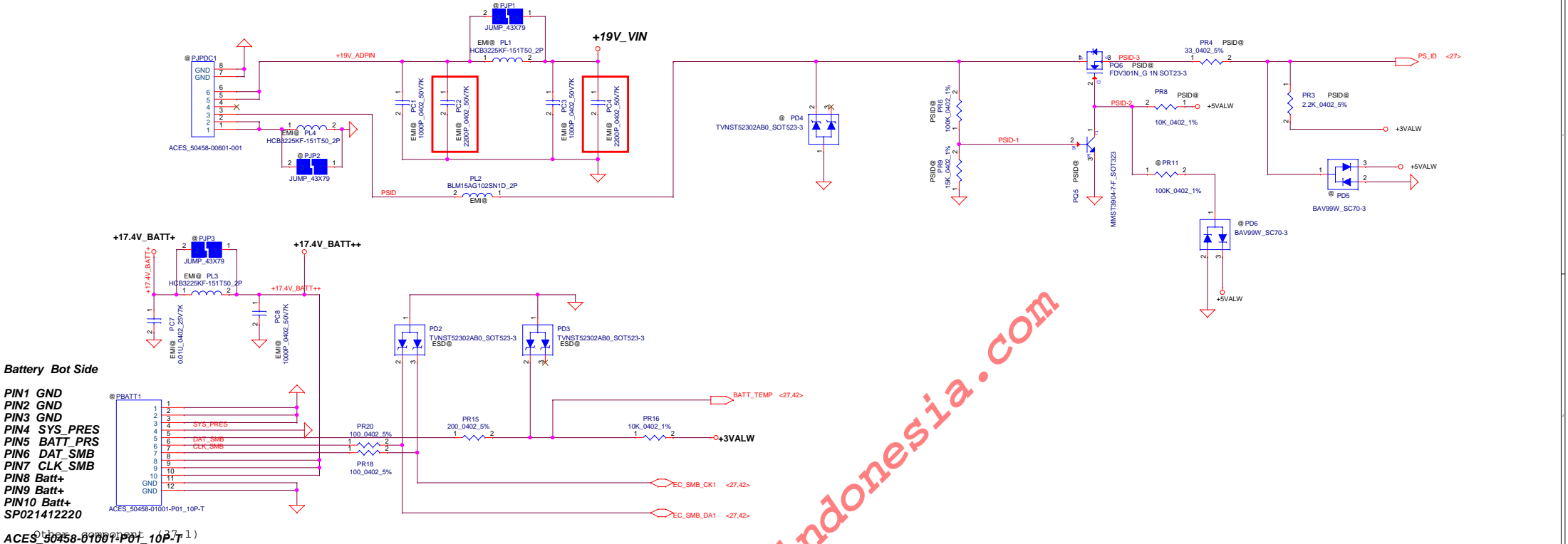
R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R16M-M30/M70 VRAM Only

Memory ID	P/N	Vendor	Description	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	2GB
110	SA00009U10L	Hynix	S IC D5 256M32 H5GC8H24MJR-R0C BGA 170P	2GB
111	SA00009TV0L	Micron	S IC D5 256M32 MT51J256M32HF-70-A FBGA	2GB

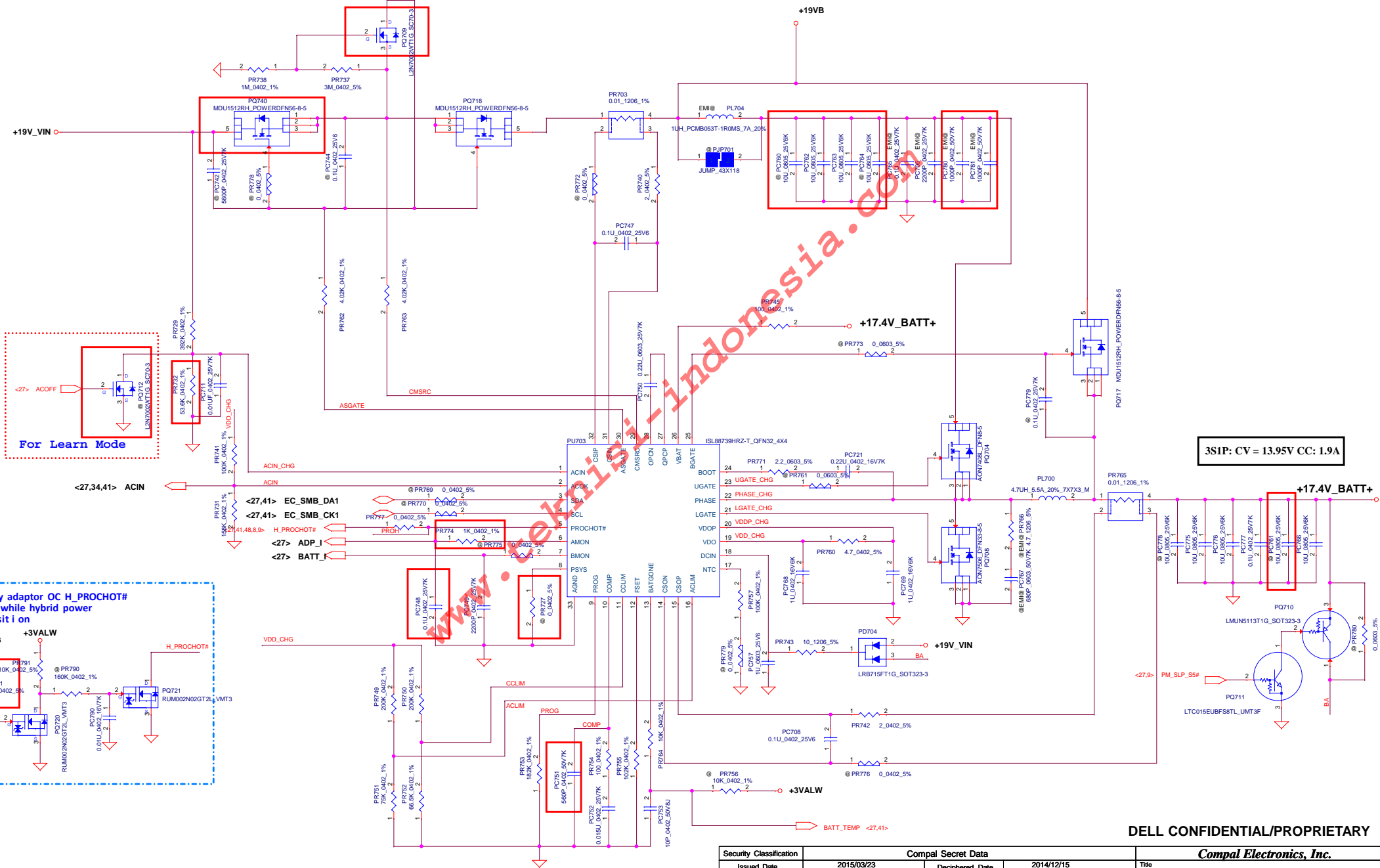
Update on 3/24



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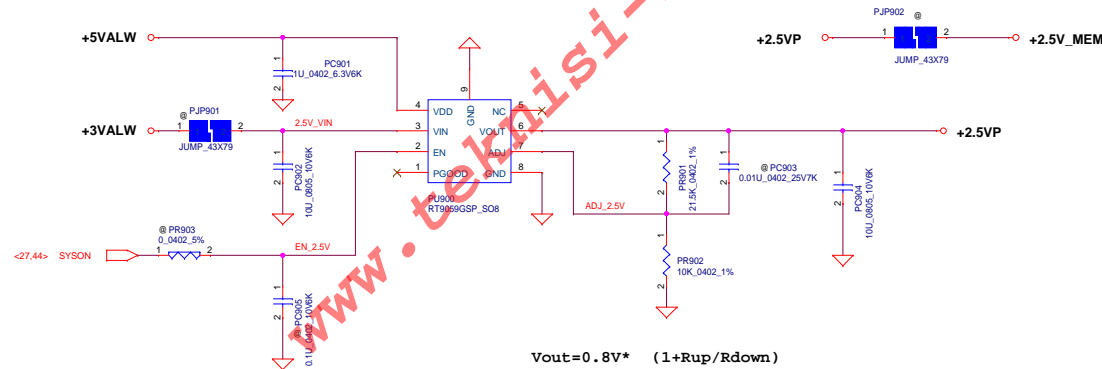
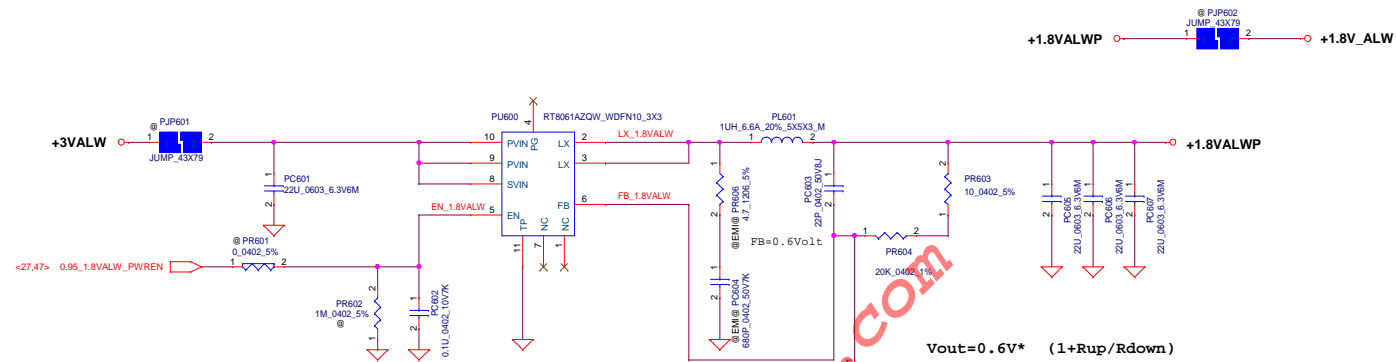
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I_{ada}=0~2.30A(45W)

$$ADP_I = 32 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$


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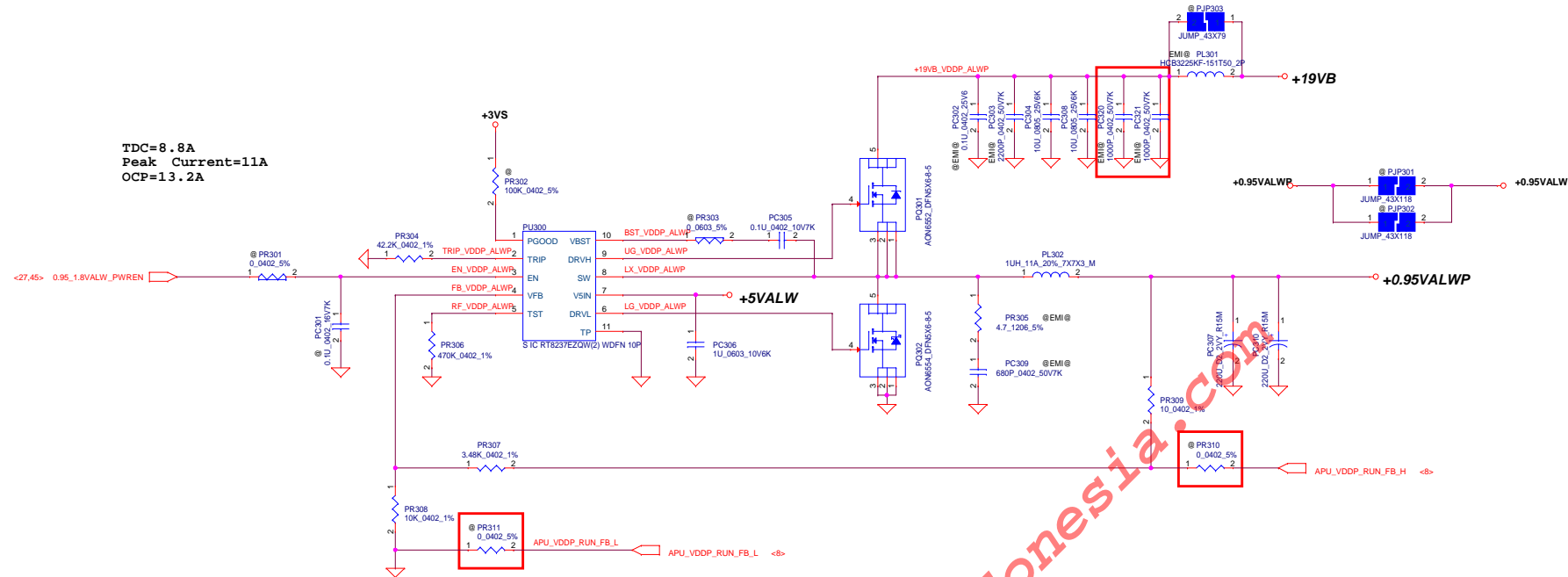
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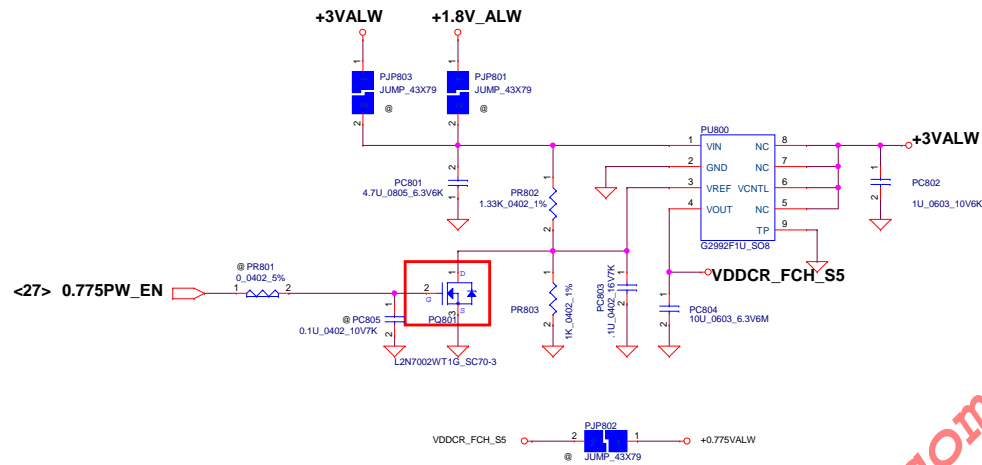
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TDC=8.8A
Peak Current=11A
OCP=13.2A



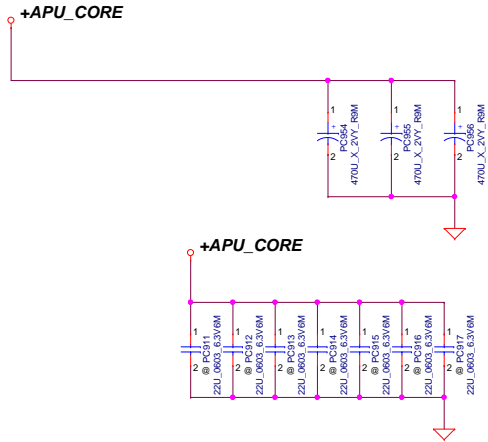
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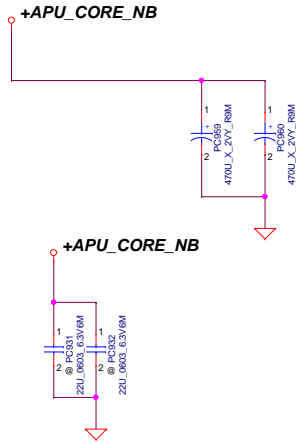
+APU_CORE

APU_CORE
470uF*3

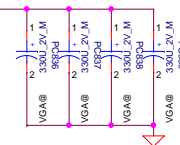


+APU_CORE_NB

APU_CORE_NB
470uF*2



+VGA_CORE

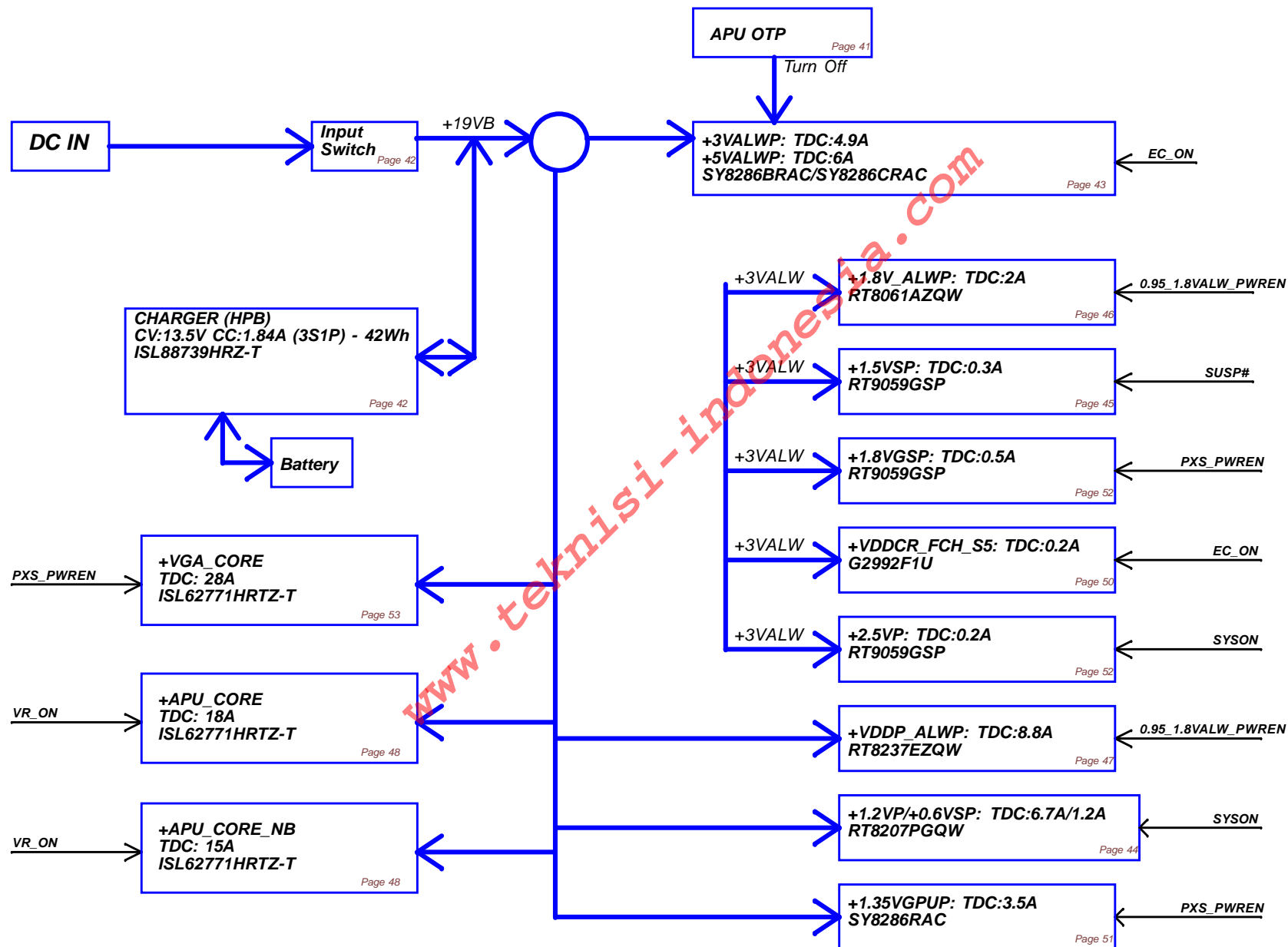


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Power block



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change power rail from 1.5V to 1.8V by EE side	delete all 1.5VS component
design change to adjust APU_CORE setting	delete PC1010 change PR1005 from 11.5K to 11.5K change PR1078 from 95.3K to 95.3K
design change	delete PR310, PR311
design change from EE recommend	add PR119 100K
adjust OTP setting from thermal recommend	change PR24 from 14K to 16K
design change to remove Erp lot6 circuit	delete PR2, PR5, PR7, PR10, PQ10
adjust OCP setting	change PR205 from 8.25K to 8.25K
design change	change PQ740 from SB000014 to SB000014
design change from EMI recommend	change PC2, PC4 from 0.1U to 0.1U
design change	change PR103 from 499K to 499K
adjust OCP setting	change PR24 from 16.9K to 16.9K

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HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
1	26	1/28	0.2	Modify the capacitor value	C621 change 1uF capacitor to 4.7uF , C620 change 4.7uF capacitor to 1uF
2	26	1/28	0.2	Part count reduce	C344 Bom structure change to " DIS@ "
3	9	1/28	0.2	Modify Resistor value	RC346 47k ohm change to 22k ohm (SD028220280)
4	30	1/28	0.2	Modify PCB Part number	Modify PCB part number to DA6001LB000
5	13	1/29	0.2	Change Capacitor to H1.9	CD229 Change to SGA20331E10
6	26	3/13	0.2	Modify RC Delay for +1.8VGS	1.8VGS_0.95VSDGPU_ON connect to U15.3 & U15.5
7	9	3/13	0.2	Reserve RC938	RC938 change to unpop
8	24	3/15	0.2	Pop Q9 for touch-pad (PTP)	Q9 Change to pop
9	16	3/15	0.2	BOM change to cost reduce	+LCDVDD power switch U1 change to SA000079400
10	11.18	3/15	0.2	Audio codec change to +1.8VS to cost down +1.5VS LDO	Add RC18/RA15/RA16 ,reserve +1.5VS
11	24	3/15	0.2	JKB1.30 remove KB_DET# (follow Tulip)	Add RE60 reserve to +5VS
12		3/16	0.2	Part count reduce	Change to R-short RC119,RA1,RA2,RA4,RA5,RL5,R16,RC53,RC52
13	10.25	3/16	0.2	Change I/O USB conn. Port (AMD request)	USB20 Port7 change to Port2
14	22	3/16	0.2	SATA net name modify	Modify to SATA_TX_P0/N0 SATA_RX_P0/N0
15	22	3/16	0.2	Remove SATA ESD	Delete EU3101
16	17	3/18	0.2	For layout request swap RP12 pin	Swap RPI2 pin
17	9	3/18	0.2	Modify BIOS strap pin	Net name vram size/APU_ID/Panel size_ID change to VBIOS_ID1/ID2/ID3
18	23	3/21	0.2	Change USB3.0 EMI choke to pass EA test	LU1/LU2/LU4/LU5 SM070003Z00 change to SM070004K00
19	29	3/21	0.2	Change power on switch part number	SW1/SW2 change to SN10000B310
20	26	3/21	0.2	Modify to meet the GPU power sequence	Modify R438 1K to 33K ohm (SD028330280)
21	30	3/21	0.2	ME drawing add a screw hole	Add H13 H_6P0 screw hole
22	24	3/21	0.2	BOM change to cost reduce	F3 BOM SP040002400 change to SP040002B00
23	30	3/21	0.2	DFx review stand of f pad can't place via	H11 H_3P2-G modify to H_3P2
24	17	3/21	0.2	For layout swap RPI1 pin	Swap RPI1 pin
25	18	3/21	0.2	Vendor feedback have extra pull-up Resistor same funct i on as RA25/ RA26	Remove RA46, RA47
27	29	3/21	0.2	Remove PWR/Board unused pin	Remove JPWR1.4 +5VALW net name
28	19	3/22	0.2	Design change for Hi-pot test fail at EVT	LANGND Change to GND
29	26	3/22	0.2	Reserve 0.1uF for +0.95VSDGPU output	Add C625 0.1uF
30	9	3/22	0.2	Reserve BIOS strap pin	VBIOS ID1/ID2/ID3 change to RESERVE_1/APU_ID/RESERVE_2
31	27	3/22	0.2	Board ID update to DVT1 Set t i g	RE22 change to 200k_0402_1% (SD034200380)
32	29	3/22	0.2	ESD request to pop	Pop EC2902 ,EC2901
33	29	3/22	0.2	Update JPWR1 Footprint	Update JPWR1 footprint "ACES_51678-00601-W01_6P-T"
34	18	3/22	0.2	Add Audio codec ALC3234 Part number	add ALC3234 PN "SA000076U00"
35	27	3/23	0.2	EC/BIOS comment no use	Unpop RE40,RE44,RW9,RW10
36	16	3/24	0.2	Sourcer request change main source	LX1 change main source to SM01000EJ00
37	40	3/24	0.2	VRAM Strap pin set t i g update	Modify BOM structure 2G_S@ ,2G_H@ ,2G_M@
38	11	3/24	0.2	For PWR to add MLCC*9	Unpop CC1117,CC1120,CC1121,CC1122,CC1123,CC1125,CC1127
39	22	3/25	0.2	SATA Parade Re-driver EQ set t i g to default 12.28	unpop RS22,RS27,RS28,RS37
40	26	3/25	0.2	Pop 0.1uF for +1.8VS & +0.95VSDGPU output	Pop C26,C625

HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
41	30	4/21	0.3	Increase EMI MLCC Cap voltage rat i ng	Change C35,C36,C37,C38,C39,C40 to SE00000G880
42	16	4/24	0.3	Increase Cap. voltage rat i ng	Change C4 10u_ 6.3V to 10u_ 25V voltage rat i ng
43		4/24	0.3	Increase Cap. voltage rat i ng	Change C34,C2305,C2306,C2308,C2323,CA1,CA3,CU13,CU18,Cs15 10u_6.3v to 10u_10v voltage rat i ng
44	18	4/24	0.3	Increase Cap. voltage rat i ng	Change CA11 4.7u_ 6.3V to 4.7u_ 10V voltage rat i ng
45	24	4/24	0.3	Increase Cap. voltage rat i ng	Change CF4 22u_ 6.3V to 22u_ 10v voltage rat i ng
46	30	4/25	0.3	ME drawing modify screw hole	Modify H6 5P0N to 5P6N
47	18	4/25	0.3	Change Part from EMI request	LA3,LA4,LA5,LA6 "SM01000BV00" change to "SM01000NX00"
48	34	4/25	0.3	Part count calculate	Change RV158,RV159,RV164 BOM structure to DIS@
49		4/29	0.3	Part count reduce	Change to R-short RC458,RC32,RC22,RC665,RC1675,RC18,RD25,RD28,RD29,RX7,R13,R6, R14,R51,R7,RA15,RA42,RA11,RA22,RL9,RW11,RA40,RE338,R37,RE5,RE31,RE32, RE33,RE34,RE37,RE38,RE50,RE51,RE42,RE39,RV164,RV27,RV30,RV31,RV364
50	8	4/29	0.3	Part count calculate	Change RC29,RC23,RC664 BOM structure to @
51	27	5/3	0.3	Board ID change to DVT2	RE22 change to 240k_0402_1% (SD000001B80)
52	6	5/3	0.3	Add AMD Stoney A9-9400 BOM	Add A9-9400 Part number SA0000A280L
53	27	5/3	0.3	ESD request to pop	Pop CE23
54	30	5/3	0.3	EMI request to unpop MLCC Cap.	Unpop C35,C36,C37,C38,C39,C40,C41,C42,C43,C44,C45,C46,C47,C48,C49
55	21	5/3	0.3	EMI request to change part	LA8,LA9 Change to 0_0402_5%
56	29	5/3	0.3	ME Update JPWR1 Footprint	Update JPWR1 footprint to "JXT_FP226H-006S1BM_6P"
57	9	5/3	0.3	APU_ID Modify BOM structure	E2A6@ Change to E2A6A9@
58	6	5/3	0.3	Add E2-9000/A6-9200 PR sample PN	Modify E2-9000 "SA00009W80L" , A6-9200 " SA0000A2A0L"
59	22	5/3	0.3	Add TI re-driver EQ set t i ng (7dø	Pop RS33, RS34 to 4.7k_0402_5% , pop RS18,RS22,RS23,RS27,RS28
60	9	5/26	1.0	Reserve 0ohm for APU_PCIE_WAKE#	Add RC967 for APU_PCIE_WAKE# (unpop)
61	26	5/26	1.0	Modify +0.95VSDGPU & +1.8VGS slew rate to meet GPU sequence	C343,C344 change to 2200pF (SE075222K80)
62	27	6/6	1.0	Board ID change to X build set t i g	RE22 change to 270k 1% ohm (SD00000G280)
63	9	6/6	1.0	Change BIOS APU_ID strap pin	RC708->A6A9@ , RC707->E2@
64	29	6/6	1.0	Reserve MB power bot t on(S_W1, S_W2)	SW1 ,SW2 change BOM structure to @
65	6	6/6	1.0	Add AMD Stoney CPU R3 PN	Add Stoney E2-9000 ,A6-9200, A9,9400 R3 PN
66		6/13	1.0	DFB issue : co-lay un-used pin need to solder mask	RI1,RI2,RI4,RI5,RI7,RI8,RI10,RI11,RU1,RU2,RU3,RU4,RU5,RU6,RU7, RU8,RU9,RU10,RU11,RU12,RU13,RU14,RU17,RU18,R17,R18 solder mask
67	24	6/14	1.0	Change JKB1 Footprint(DFB issue)	Change JKB1 Footprint to use SP01001LN00 footprint (2nd source)
68	18	6/14	1.0	EMI part count reduce	RA17,RA18,RA19,RA20,RA21 0ohm Change to R-short
69	24	6/14	1.0	Add GPU R3 PN	Add AMD M1-30 R3 PN
70	24	6/14	1.0	Add VRAM R3 PN	Add VRAM Samsung , Hynix, Micron R3 PN
71	30	6/15	1.0	Add PCB R3 PN	Add PCB R3 PN "DA6001LB011"
72	11	6/16	1.0	Extra 0.22uF Cap. , Follow AMD checklist	CC1129 Change Bom Structure to @